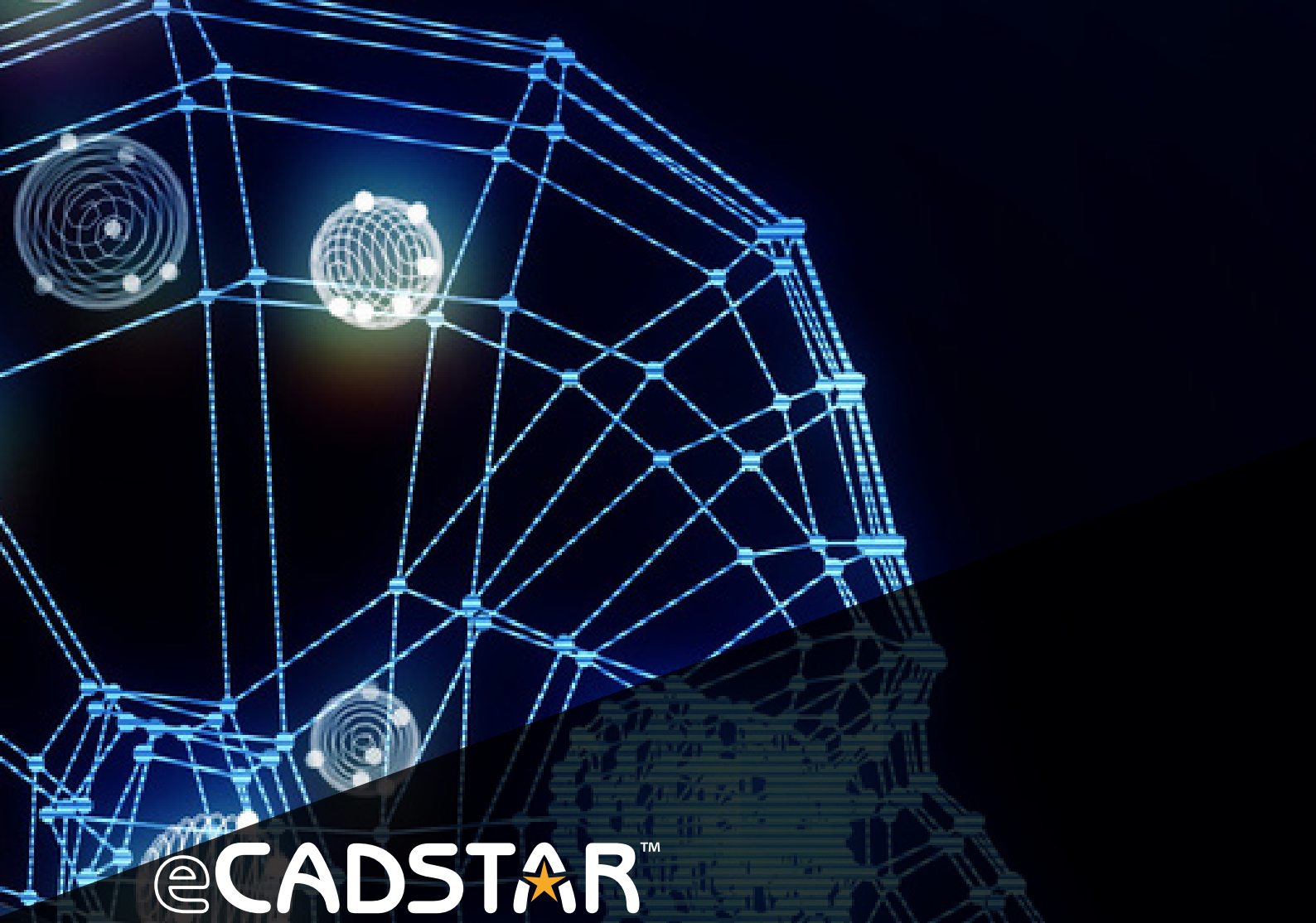

eCADSTAR™

DATASHEET

IBIS-AMI

The IBIS Algorithmic Modeling Interface (AMI) is a modeling standard for SerDes PHYs, that enables a fast, accurate, statistically significant simulation of multi-gigabit serial links. IBIS-AMI was developed as extension to standard IBIS models by the IBIS Open Forum, a consortium of EDA, semiconductor and systems companies. This has been part of the IBIS standard since Rev 5.0.

While traditional IBIS models describe the IC buffer driving and receiving characteristics, they cannot include any description of programmable (DSP like) behavior like those present in IC communication architectures in PCI Express Gen3, USB, SATA, DisplayPort and others.

WHY DO YOU NEED AMI SIMULATION?

- AMI models are needed to simulate advanced transceivers like those in PCI Express (PCIe), SATA, USB3 etc. These transceivers use Digital Signal Processing (DSP) techniques like pre-emphasis and equalization to condition signals for ultra-high bitrates and to compensate for interconnect losses.

- High-speed serialized data operating with very low voltage swings is very sensitive against attenuation in the channel. Higher-level verification with long stimulus patterns is essential to find key performance parameters like a low Bit Error Rate (BER) which is required by the protocol of these interconnect schemes. Waveform simulation cannot predict this behaviour, so advanced analysis techniques like AMI simulation are needed.

- Since AMI models include the programmable behaviour of the PHYs in their algorithmic part, you can adjust parameters to optimize I/O channels for maximum performance. This is often the only way to validate channels in a pre-production environment, it as well increases the margin for unexpected post-production issues like poor operating environments and external electrical noise.

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AMI analysis goes beyond traditional waveform simulation, as IBIS-AMI models include conventional analog elements and algorithmic descriptions too (compiled code), they can run much faster in dedicated SI simulators like the one in eCADSTAR than for instance traditional SPICE models (up to 1 million bits/minute).

BASIC STRUCTURE OF IBIS-AMI MODELS

IBIS-AMI models comprise two main elements:

- The Analog part, just as in traditional IBIS, includes things like the component pin-definition, package parasitics, basic voltage/current curves and input capacitance values, expressed in textual form.

- Algorithmic models, implemented using Dynamic Linked Library (DLL) code.

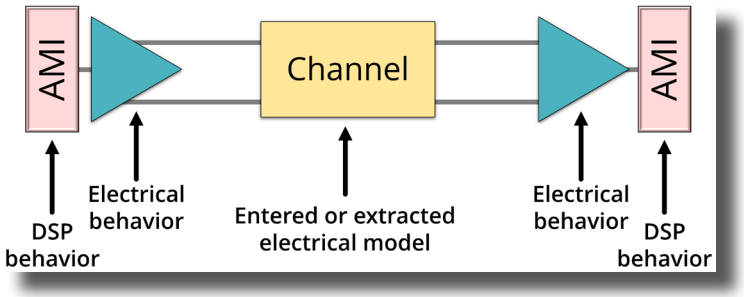

FIGURE 1: Basic structure of an IBIS-AMI model

If for example, you were modelling a differential PCI Express TX signal, the models of the output could include their internal DSP behavior if the model maker (mostly the IC vendor) has included these into the AMI model.

The simulator GUI then reveals access to the programmable elements of the AMI model, allowing you to tune parameters for the channel simulation similar to how a real chip can be tuned by setting various hardware registers.

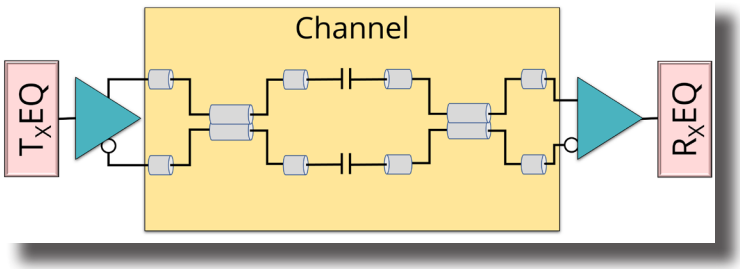

FIGURE 2: PCIe TX signal where both analog and algorithmic buffer models are required

IMPORTING IBIS-AMI MODELS

Import IBIS-AMI models into your simulation library just as you can with traditional IBIS, using Simulation Library Browser, even though the model data is very different.

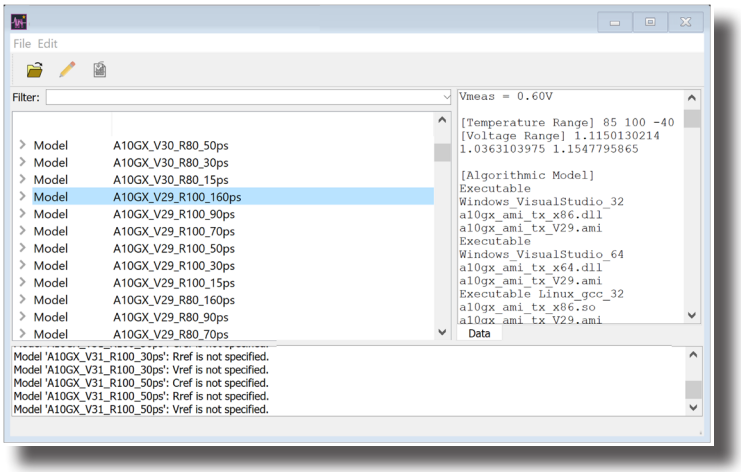

FIGURE 3: Importing IBIS-AMI models into the simulation library

ASSIGNING AMI MODELS

You can assign AMI models in Scenario Editor, launched from eCADSTAR Schematic Editor or eCADSTAR PCB Editor. These can be differential topologies extracted from schematic data, real physical layout or topologies created entirely by yourself to conduct generic pre-design studies. AMI models are for detailed channel analysis, so they are assigned here, after a transmission-line topology has been extracted, edited or drawn, rather than directly to components within the design.

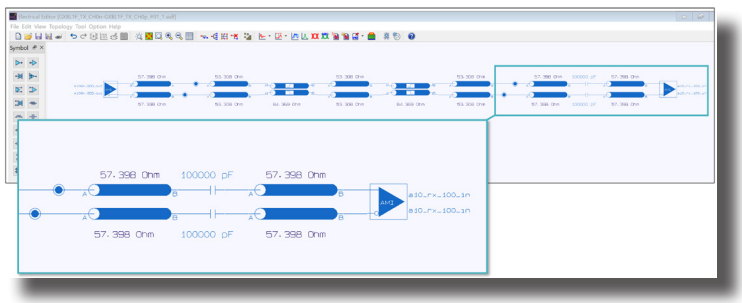

FIGURE 4: AMI models assigned to buffer symbols

CHANNEL CHARACTERIZATION AND SETTING UP AMI ANALYSIS

Prior performing a channel analysis the transmission behavior of the channel can be checked by optional characterization steps, evaluating the frequency domain response resulting in S-Parameters and the transfer function, but as well the time domain impulse response of the channel. There are comprehensive initial steps to verify channels to the standards you want to meet.

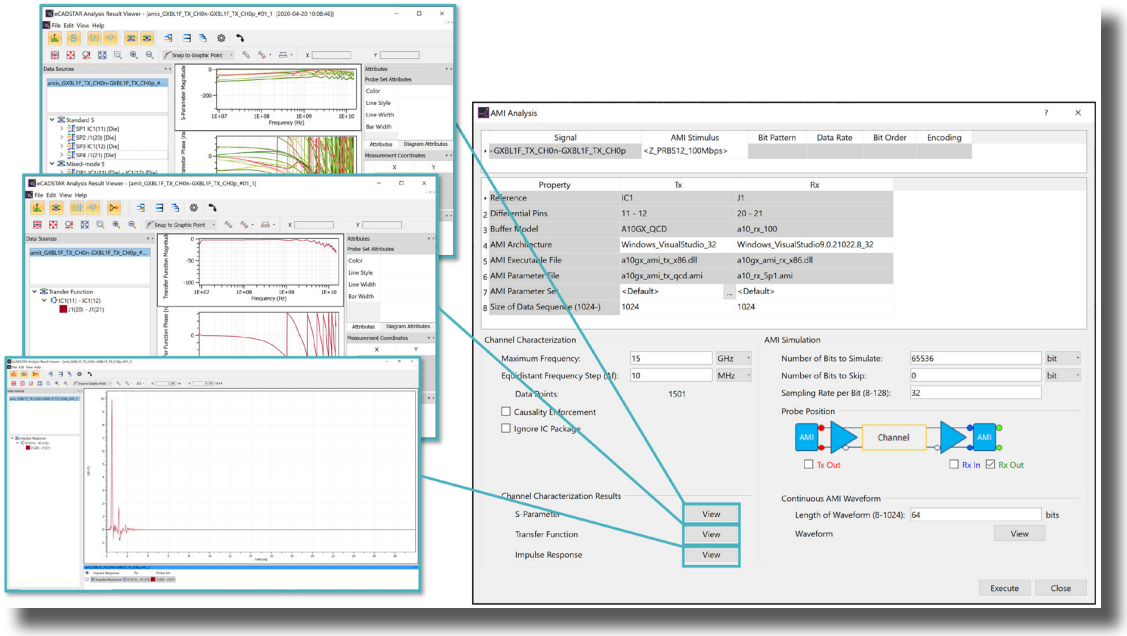

FIGURE 5: Characterizing a high-speed channel and setting up for AMI simulation

Key channel characterization results include:

- S-Parameter analysis.
- Transfer function.
- Impulse response.

SIMULATING TO DETERMINE KEY CHANNEL PERFORMANCE DATA

It's important to know expected channel performance, because optimized I/O enhances the performance of your entire product. Key parameters such as Bit Error Rate (BER) are presented clearly.

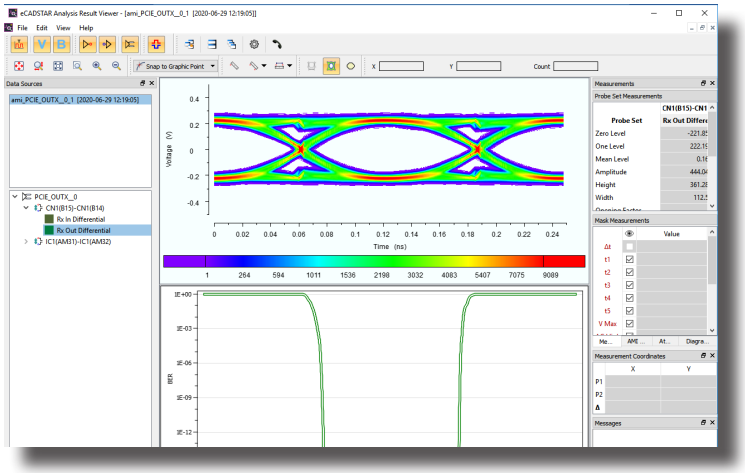

FIGURE 6: AMI simulation result showing Bit Error Rate (BER)

Results include:

- Eye pattern analysis with optional measurements against eye mask.
- Jitter.
- Bathtub curve to check Bit Error Rate (BER) requirements compliance.