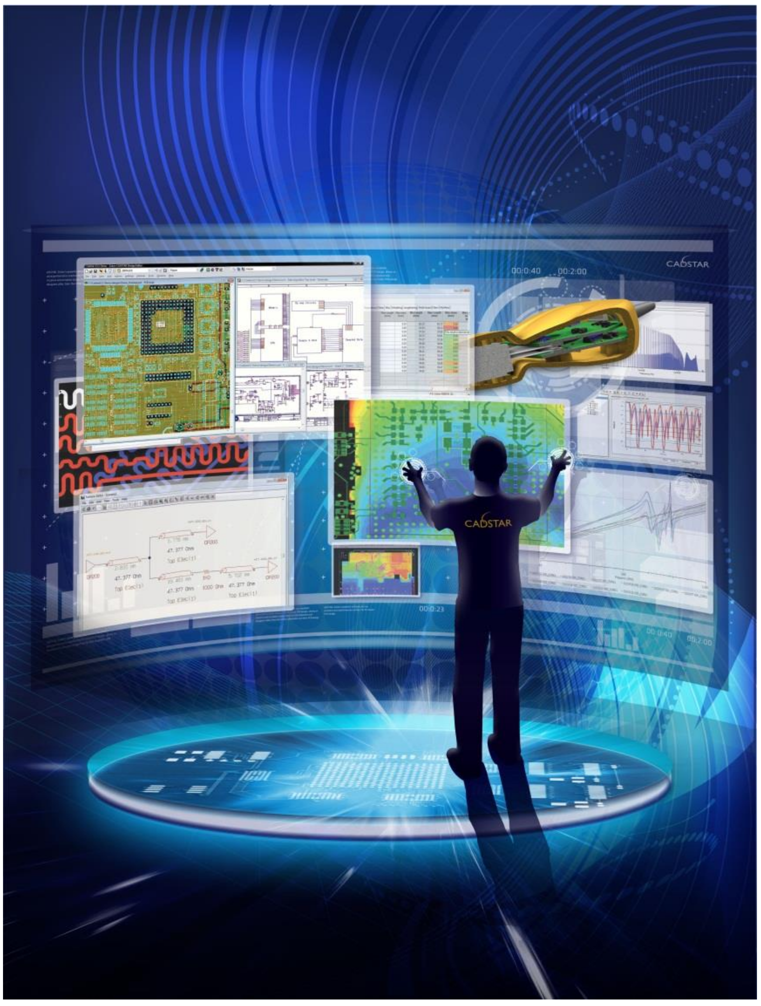
# CADSTAR Express



Do-it-Yourself Training Guide

ZUKEN®

# Express
# Do-It-Yourself Guide
# With Projects for Training Purposes

## Welcome!

Thank you for acquiring CADSTAR Express. This free version provides a number of features used in the full CADSTAR version, only limited by the number of components (max 50) and pins (max 300).

Electronic hobbyists, Students and Evaluators use CADSTAR Express for designing Schematics and Printed Circuit Boards (PCB). This guide will assist you in detail on how to make use of CADSTAR's features to design your next project.

- We will start by showing you a hand drawn electronic circuit and transforming it into a professional schematic design.
- We will guide you through the process of creating an error-free transfer of data to a PCB board design, and then move to component placement and wire routing.
- You will then move to the CAM output process where you will generate the necessary artwork, reports and files needed to get your PCB built by your preferred fabrication vendor.
- We will guide you through the process of creating schematic symbols, component and parts for future CADSTAR libraries.

Upon completion of this guide, you will be ready to move into higher variations of CADSTAR, offering features and constraints for High Speed signal applications and simulation as well as 3D Electro-Mechanical collaboration.

To provide you with additional "how to" information, click on the camera icons for demonstration videos. (internet connection required)

**The videos are for demonstration purposes only. They are not created to match the exact instructions in the task steps. Please follow the specific steps in the tasks.**

When CADSTAR Express is executed this PDF Document will appear for your convenience. If you have not installed CADSTAR Express, simply double click on the executable for set-up and follow the instructions.

**As you work through the tasks in this guide, you will be instructed to save files with suggested file names. If you do not finish a task and simply wish to move on to the next task, back-up files are supplied for your convenience. Files with the "_CS.*" suffix can be opened and then saved using the *File→Save as* function to overwrite the file you are working on.**

Enjoy!

CADSTAR

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**Please Note: This do-it-yourself guide has been revised using a Windows 10 environment. The software has been installed on the author's computer using the default locations and selections per the CADSTAR Express SETUP program. CADSTAR Express is also supported using Windows 7 and 8.**

Last updated : 05 September 2019

## Introduction to CADSTAR

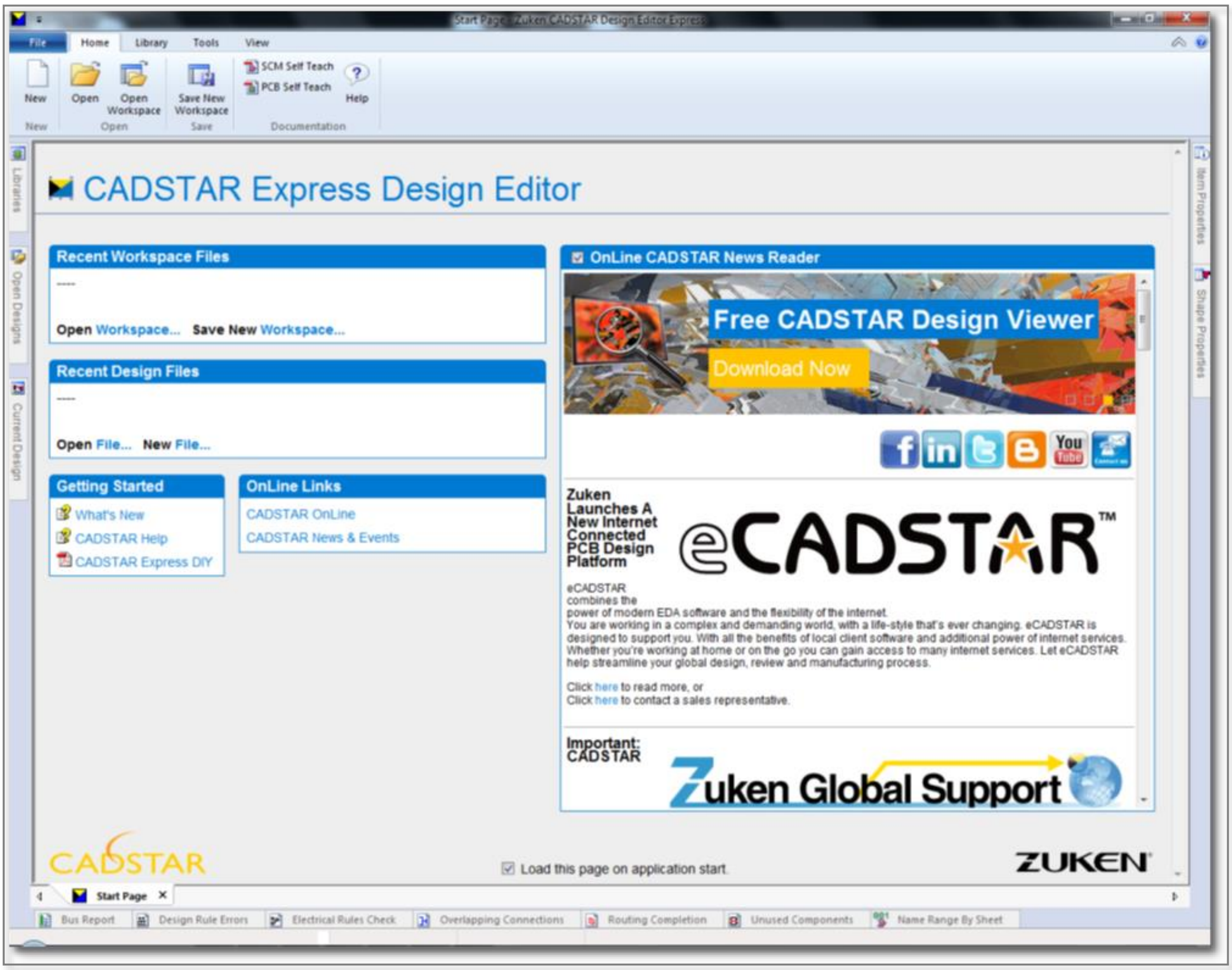
CADSTAR is an EDA design tool allowing you to draw schematic designs and transfer them to the PCB layout environment. After an error-free transfer, CADSTAR helps to place the components into the board outline.

Placement and Routing is an integral part of a PCB design process. CADSTAR offers much flexibility in this area by providing both Push-aside Placement and Routing tools (manual, semi-automatic and fully automatic) within the Embedded Place & Route Editor or the advanced standalone Place & Route Editor. The Embedded Place & Route Editor has been developed in general for basic PCB design or users who don't use a PCB design tool regularly, and the standalone Place & Route Editor is for the more advanced users who require more powerful functions. For really advanced users (industry users) high-speed design features (such as lengthening, delay, impedance, cross-talk, overshoot, reflection etc.) can also be provided in a full standard package or as an optional add-on. The additional add-ons that are available to you, include ***BoardModeler Lite*** which is a *unique* 3D verification tool for PCB design that provides a completely new concept of PCB Design in a 3D environment or the CADSTAR Variant Manager which enables you to generate variants of a 'master' design (included B.O.Ms and assembly drawings) without having to maintain separate files for each variant.

The completion of the PCB design is followed by the generation of manufacturing output data for PCB fabrication.

## Getting Started

By now you have probably installed CADSTAR on your PC and are anxious to get started. Start by clicking the **Design Editor** Icon in your ***Start→All Programs→CADSTAR Express XX.X*** menu. When CADSTAR is started you will see the **Start page** as shown below.




It allows you to;

- Access recently opened Workspace Files.
- Access recently opened Designs.
- Access Help and PDF files.
- Read up on the latest in CADSTAR News from the World of Zuken.
- Access some On-line Links such as the CADSTAR Web pages.

CADSTAR is a Multi-Document Design Environment. Soon you will have schematic designs and PCB designs all open in the same *Design Editor* environment.

## The Basic Design Flow

**Library** Usually you need to start off with a library to ensure that all the parts (schematic symbols & PCB footprints) required for your design are available to you. However, to complete the exercises in this guide, all parts have been provided. When you are ready to create new parts in the CADSTAR library, please study chapter 3.

**Note:** the library provided with CADSTAR Express contains all the parts required for the PCB designs described in this 'Do-It-Yourself" guide as well as some examples from the on-line CADSTAR Libraries. (**Accessing the CADSTAR On-line libraries requires a higher variation of CADSTAR and an active maintenance contract**).

**Schematic** It is always advisable to start with a schematic design before moving onto the PCB design, although CADSTAR does support reverse engineering with full back annotation capabilities.

**PCB (Placement)** After the successful transfer from schematic, components will be placed within the board outline and respective placement areas.

**PCB (Routing)** After placing all the components, we can start routing the critical nets manually and/or through automatic routing.

**Manufacturing Output** The final stage of any PCB design. No matter what your manufacturer requires, CADSTAR can deliver; extended Gerber (RS274X), extended N.C. Drill (Excellon), Placement data, Bill of Materials, IPC356-D test data, DXF and ODB++

## The User Interface

CADSTAR is very easy to use! The User Interface is very consistent in operations whether you are editing a Schematic or a PCB Design.

CADSTAR Supports;

- *Ribbon style* Tool bars can be dragged and docked as needed
- Tool bar Icons that can be allocated as the user wishes
- Customizable Tool bars and Menus are supported for adding user defined reports and Macros
- Tabbed Document Window support – Most often seen in more modern version of Windows 10 and MS Office ®
- "Strokes" - command macros that perform the most common functions for panning and zooming
- Omnidirectional panning by depressing the middle mouse button or <M.M.B.>
- Themes to alter the appearance of CADSTAR when working in a more modern operating system, "Windows 10", such as Collapsible Menus for a more condensed menu appearance
- Active HTML reports – Active HTML reports can be placed anywhere just like any other dockable window in CADSTAR. The reports you currently have open will appear as tabs in the Active Report window

## Strokes in CADSTAR and the Place & Route Editor

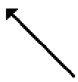
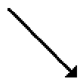
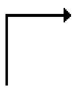
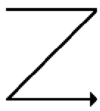
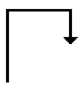
If you are not familiar with Stroke commands, you can use them for;

Indicating operations you wish the application to perform by dragging the right mouse button in the shape of one of the 'gestures' in the table below.

To make the gesture:

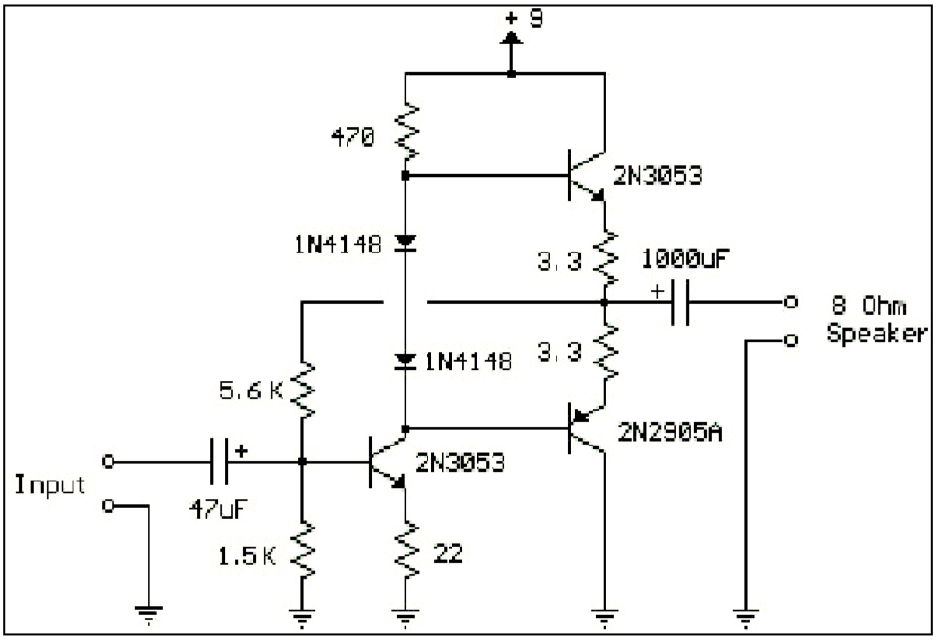
- Use the mouse to position the cursor in the design window
- Click the **R**ight **M**ouse **B**utton or <**R.M.B.**> and *Hold* while moving the mouse so that the cursor follows the path of the gesture. The application will provide feedback by drawing a white line showing the path of the cursor
- Release the right mouse button

**Note:** The shape of the path followed by the cursor is important. The direction which the cursor takes along the path is also important, since it is often true that each of the two different directions is associated with a different operation.

| Gesture | Icon | Operation | Gesture | Icon | Operation |
|---|---|---|---|---|---|
|  | | Pan up |  | | Pan left |
|  | | Pan down |  | | Pan right |
|  | | Zoom in |  | | Zoom out |
|  | | View all<br>(Display all of the drawing/design or component/symbol) |  | | Zoom to selected area<br>(the minimum box which contains both the start and end points) |
|  | | Redisplay the current view, repairing any damage to the objects displayed |  | | Zoom to selected area<br>[see above] |
|  | | Previous View<br>Revert to the view as it was before the last view-changing command such as pan or zoom | | | |

# Chapter 1 – Design A

## Introduction to the Amplifier circuit




Transistor Audio Amp (50 mW)

## Information on Design A - Transistor Audio Amplifier

Here is a little audio amplifier, similar to what you might find in a small transistor radio. The input stage is biased so that the supply voltage is divided equally across the two complimenting output transistors, which are slightly biased in conduction by the diodes between the bases.

A 3.3 Ohm resistor is used in series with the emitters of the output transistors to stabilize the bias current so it doesn't change much with temperature or with different transistors and diodes. As the bias current increases, the voltage between the emitter and base decreases, thus reducing the conduction.

Input impedance is about 500 Ohm and voltage gain is about 5 with an 8 Ohm speaker attached. The voltage swing on the speaker is about 2V without distorting and power output is in the 50mW range. A higher supply voltage and the addition of heat sinks to the output transistors would provide more power. The circuit draws about 30mA from a 9-12V supply.

## Step 1 - Schematic for Design A

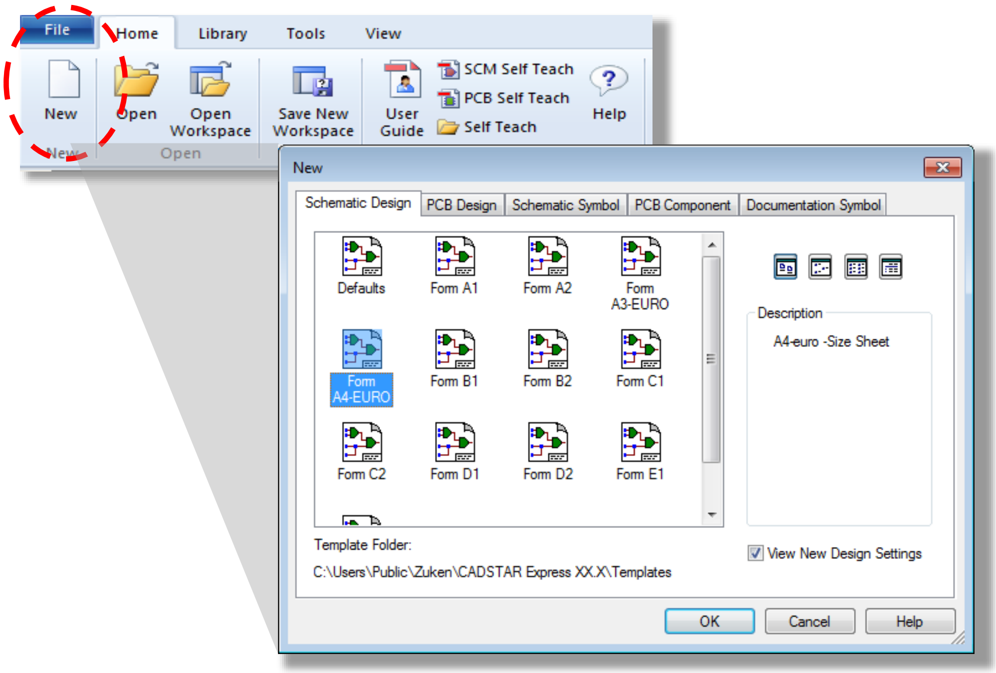
Start by reviewing the hand drawn schematic shown previously - the design of the audio amplifier. You will then have to gather the components being used in the circuit

From the hand-drawn schematic, you will find twelve (12) parts in the Library. They are;

| Qty. per | Part | | |
|---|---|---|---|
| 2 | 2N3053 NPN Transistor | 1 | 470 Ohm Resistor (470E-MRS25-1%) |
| 1 | 2N2905A PNP Transistor | 1 | 1.5 kOhm Resistor (1K5-MRS25-1%) |
| 2 | 1N4148 Diode | 1 | 5.6 kOhm Resistor (5k6-MRS25-1%) |
| 2 | 3.3 Ohm Resistor (3E3-MRS25-1%) | 1 | 47uF/10V Elec. Cap (47uF-10V-EC) |
| 1 | 22 Ohm Resistor (22E-MRS25-1%) - | 1 | 1000uF/50V Elec. Cap (1000uF-50V-EC) |
| 5 | SOLDEREYE 1MM (for Input, Speaker and 9V supply) | | |

You can use a 9V battery for this power supply.

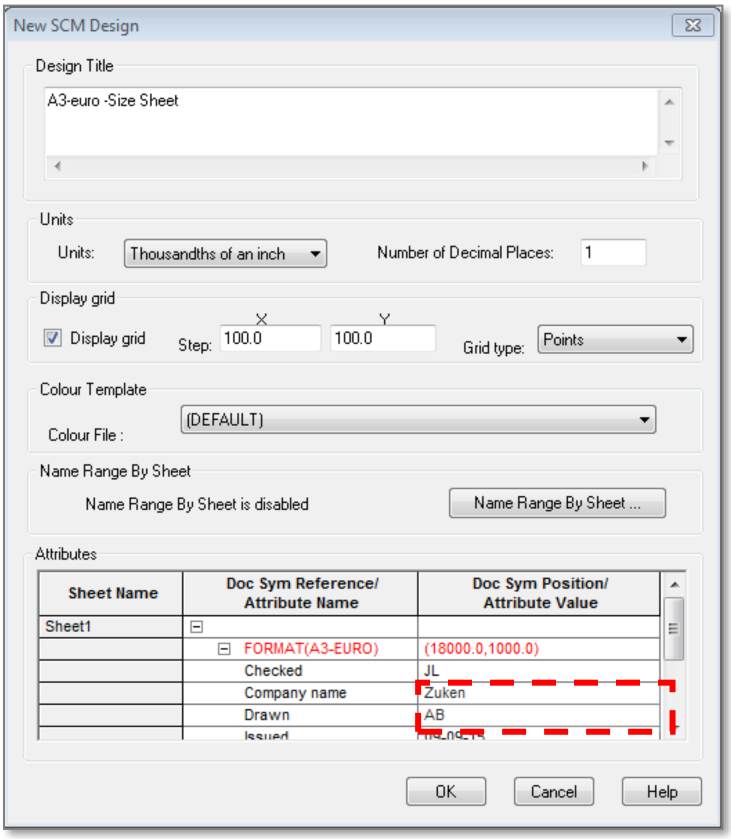
1. Click the **New** icon on the [**Home]** tab or select **[File]** tab→**New [Schematic Design**] and choose one of the templates such as ***Form A3-euro***.



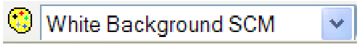

Once you select a template you are prompted with parameters to enter information using the *Attributes* that have been created for you.

2. If you like, enter your company name and personal name in the attribute fields below.

These will appear in the Title block of the Schematic format symbol. Later you can easily customize your own attributes and format sheets.

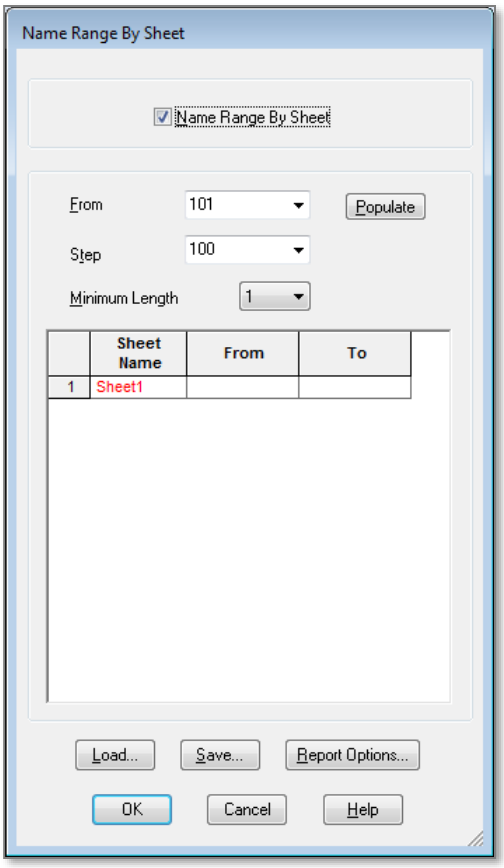



**TIP:** If you don't like to work with a black background, you can also select a different background colour scheme from the toolbar.

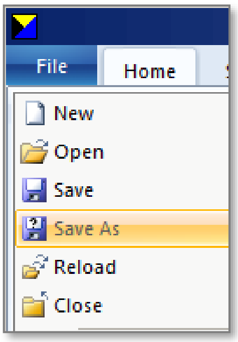



3. Click [OK]

**Note:** If you are creating larger schematics using many sheets, you may choose to declare reference designator name ranges **By Sheet**. Clicking the button shown above will display the dialog shown below. For this design we will only need one sheet.



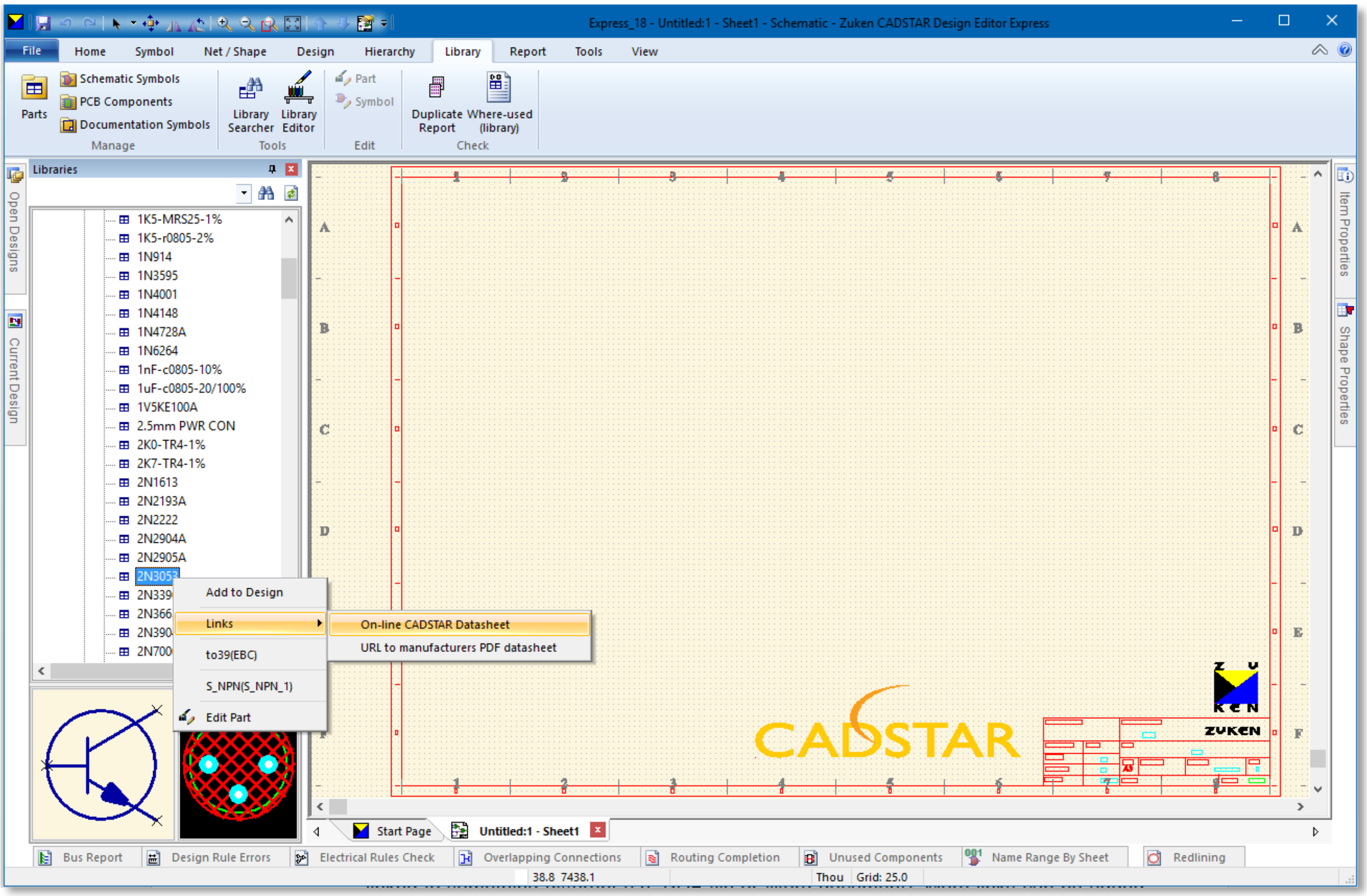

You have just started a new *untitled*, schematic design. Select the **[File]→Save as…]** Name it **DesignA1.scm**



CADSTAR

You can now start to add the parts and symbols required using the **Libraries** auto-hide panel on the left of the application window.  For a demonstration click the camera Icon.

**Note:** The Auto-hide panels for Libraries, Designs, Shape Properties, etc., can be automatically hidden if you wish. Simply click the **Auto Hide** Icon shown below. When you move your cursor off of the workspace panel it will automatically slide to a hidden position. To show the panel again, drag your cursor back to the desired Workspace panel tabs on the left-side of the application window. When it appears click the **Auto Hide** push pin icon to hold it open.

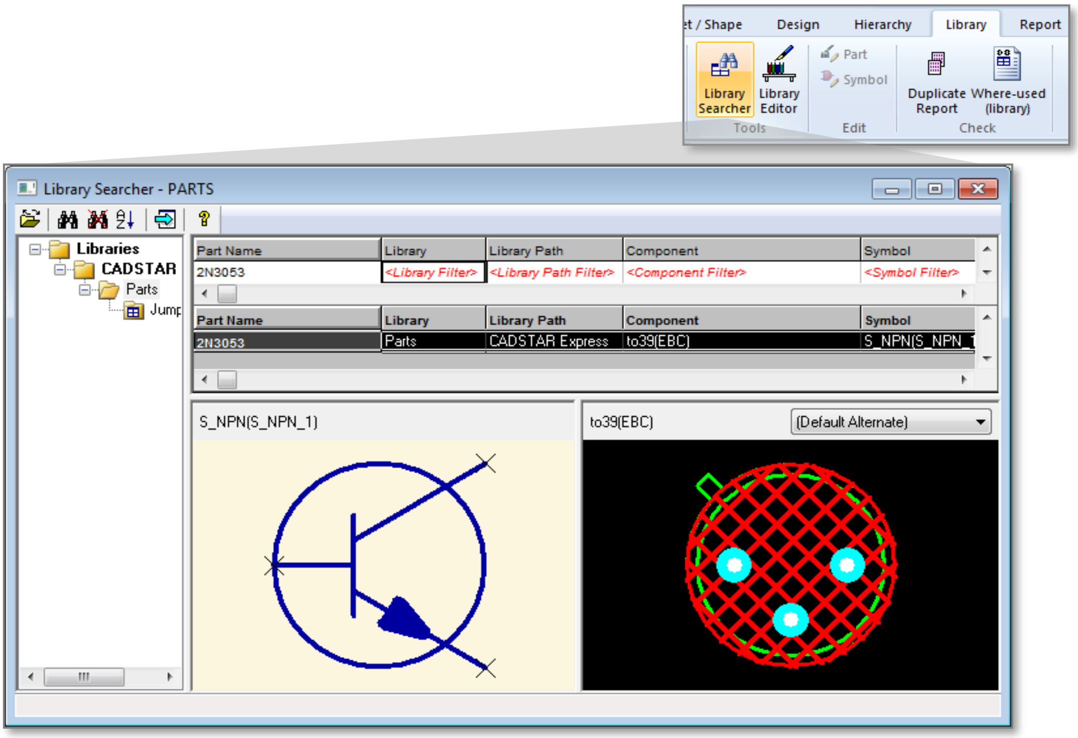



**Tip**: When adding the part/symbols into the design (like 2N3053), you can select the symbol and *click* on the right-hand mouse button <**R.M.B.**> to see a ***Link: On-line CADSTAR Datasheet***. The link is a hyperlink to a URL on the internet (or intranet), but can also be linked to something different (i.e. PDF file or Word document). More links can be added to parts in the CADSTAR Parts Library Editor. Be aware that some links might be out of date as the part may be obsolete.

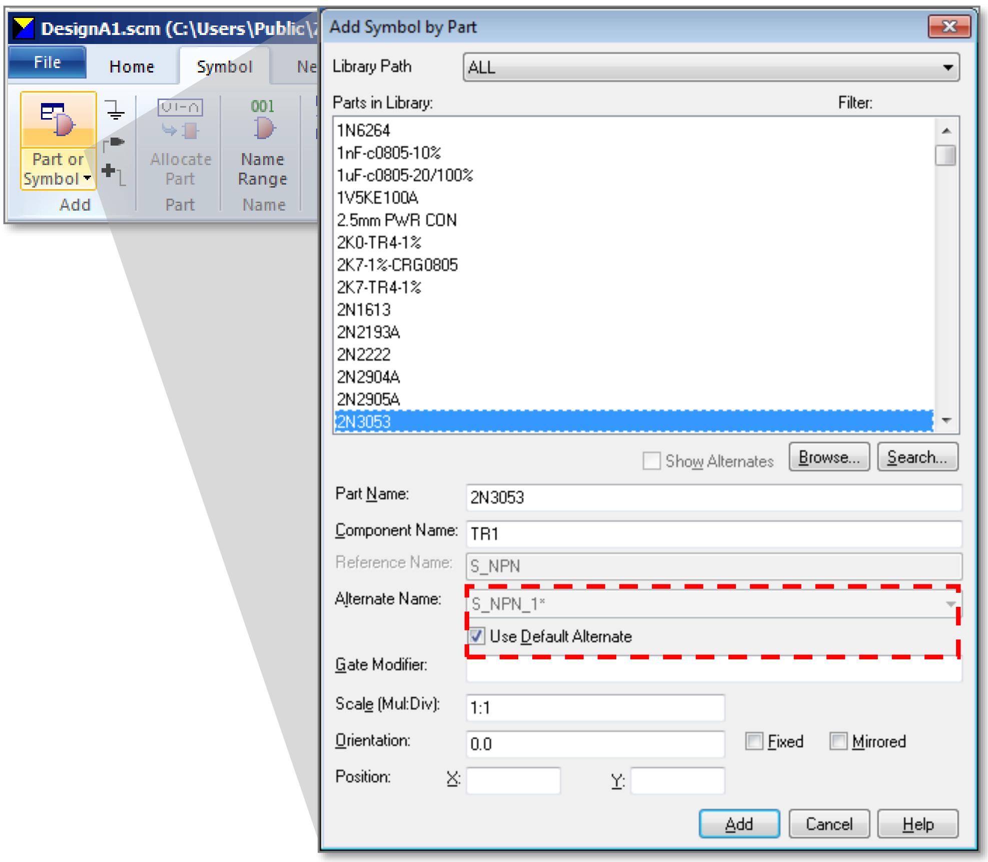
## Add Parts and Symbols

For advanced library searching and filtering try one of the additional following methods. Both allow you to specify which alternate symbol to use if available.

- From **[Library]** tab click the **Library Searcher** function. Select the **Parts.lib** *(or any of the other Parts Libraries you want to search).*



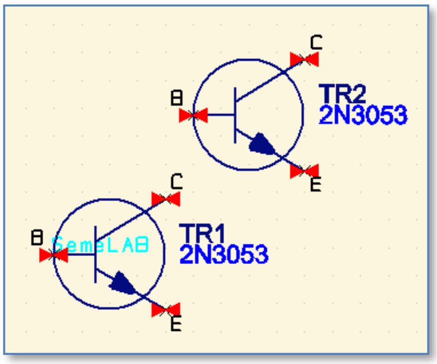

- **[Symbol]** tab →**Part or Symbol**



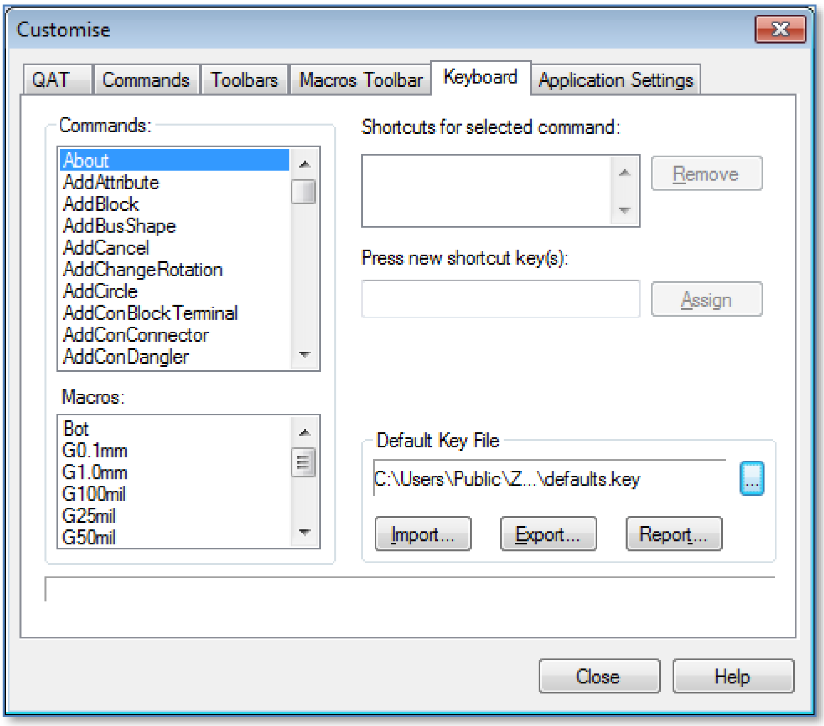
4. Place two 2N3053 transistors onto the schematic by clicking the **Add to Design** option or by dragging the transistor from the Libraries panel, i.e. highlight 2N3053 for a TO-92 package, click and hold the left-hand mouse button down, without releasing it and drag it on to the sheet.

   Don't be concerned about the red bow-tie markers on the pins. They highlight unconnected pins (the markers will disappear once you connect the pins).

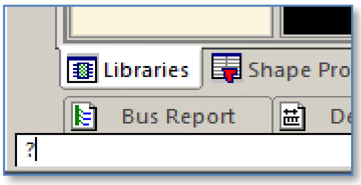
   While dragging, you can use the right-hand mouse button for mirror and/or rotation for the placement of a symbol, use the '**m**' or '**r**' hotkeys, or use a programmable function key like <**F3**> to rotate.




**Tip:** You can setup the function keys by selecting the **[File]** tab and the Customize button at the bottom, right of the menu.

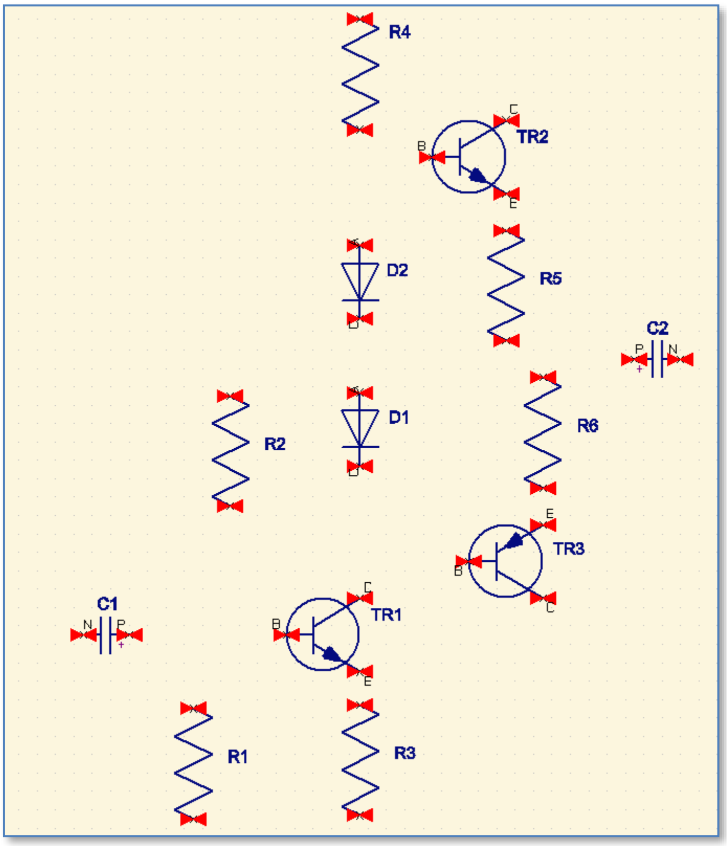



**Tip:** For more information on hot key commands type **'?<enter>**' (this will appear on the command line at the lower left corner of the application).



5. Do the same for the other 11 parts (you can either select the through-hole or SMD components):

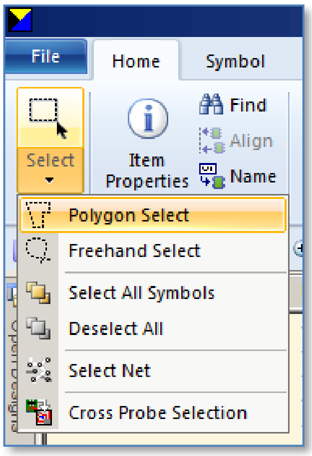
| Qty. | Part | Ref des |
|---|---|---|
| 1 | 2N2905A PNP Transistor | TR3 |
| 1 | 1.5 kOhm Resistor (1K5-MRS25-1%) | R1 |
| 2 | 1N4148 Diode | D1, D2 |
| 1 | 5.6 kOhm Resistor (5k6-MRS25-1%) | R2 |
| 1 | 22 Ohm Resistor (22E-MRS25-1%)2 | R3 |
| 1 | 470 Ohm Resistor (470E-MRS25-1%) | R4 |
| 2 | 3.3 Ohm Resistor (3E3-MRS25-1%) | R5, R6 |
| 1 | 47uF/10V Elec. Cap (47uF-10V-EC) | C1 |
| 1 | 1000uF/50V Elec. Cap (1000uF-50V-EC) | C2 |



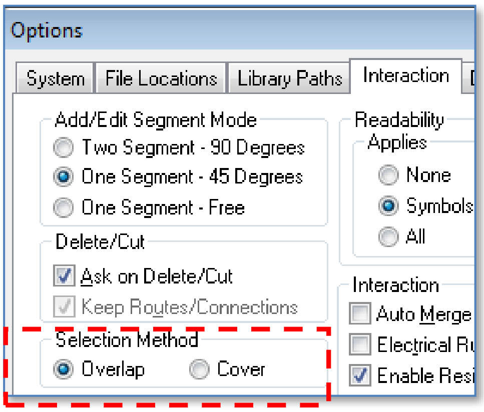

Attempt to place the parts in this arrangement.

6. You can move more than one symbol at a time. Hold down the <Ctrl> button on the keyboard and make your selections and then *Click and Drag* them.

7. Try using the **Polygon Select** and **Freehand Select** functions to select everything within an area. Select the **Home** tab and click **Select** icon to access various selection tools. Select **Polygon Select** and draw a polygon/fence around the items you want to select. When you are ready to select them double-click the left mouse button to accept the polygon or if using the freehand selection mode, just release the left mouse button and then *Click* and *Drag* them.



An additional selection method is available in the **[File]** tab→**Options**→**[Interaction]**. Here you can choose between **Overlap** and **Cover** selection methods.

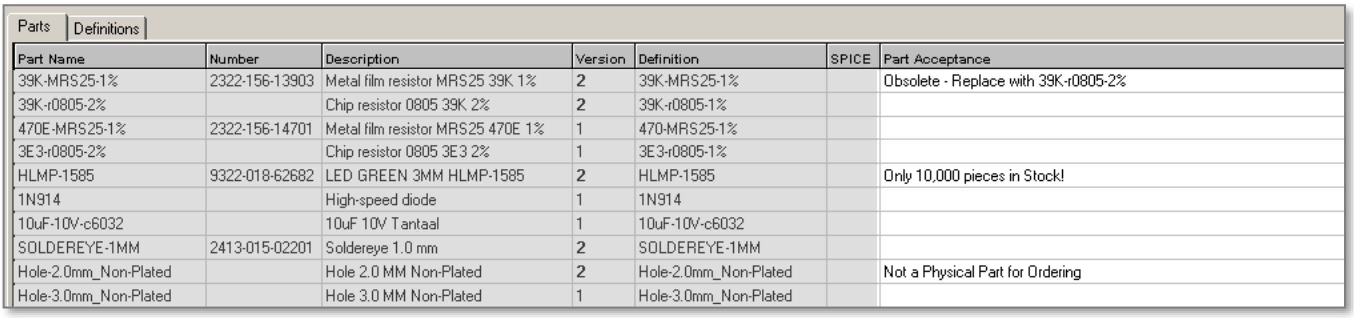



This gives more control over how items are selected during Frame Select, Polygon Select and Freehand Select.

- Use **Cover** to only select items completely covered by the selection shape.
- Use **Overlap** to select items partially covered by the selection shape.

A different cursor is displayed to show which selection method is in use. The selection method can be toggled by right clicking whilst drawing a selection shape. I.e. Holding down the **L**eft **M**ouse **B**utton and clicking the **R**ight **M**ouse **B**utton.

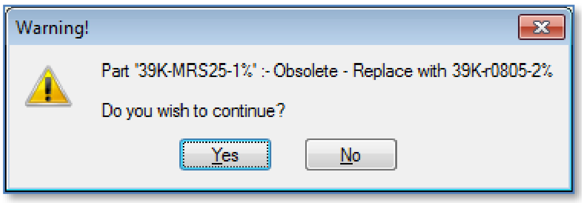
**Note:** When adding parts you be may prompted with a Warning!. This can be controlled by using a special attribute value to control "**Part Acceptance**".



| Part Name | Number | Description | Version | Definition | SPICE | Part Acceptance |
|---|---|---|---|---|---|---|
| 39K-MRS25-1% | 2322-156-13903 | Metal film resistor MRS25 39K 1% | 2 | 39K-MRS25-1% | | Obsolete - Replace with 39K-r0805-2% |
| 39K-r0805-2% | | Chip resistor 0805 39K 2% | 2 | 39K-r0805-1% | | |
| 470E-MRS25-1% | 2322-156-14701 | Metal film resistor MRS25 470E 1% | 1 | 470-MRS25-1% | | |
| 3E3-r0805-2% | | Chip resistor 0805 3E3 2% | 1 | 3E3-r0805-1% | | |
| HLMP-1585 | 9322-018-62682 | LED GREEN 3MM HLMP-1585 | 2 | HLMP-1585 | | Only 10,000 pieces in Stock! |
| 1N914 | | High-speed diode | 1 | 1N914 | | |
| 10uF-10V-c6032 | | 10uF 10V Tantaal | 1 | 10uF-10V-c6032 | | |
| SOLDEREYE-1MM | 2413-015-02201 | Soldereye 1.0 mm | 2 | SOLDEREYE-1MM | | |
| Hole-2.0mm_Non-Plated | | Hole 2.0 MM Non-Plated | 2 | Hole-2.0mm_Non-Plated | | Not a Physical Part for Ordering |
| Hole-3.0mm_Non-Plated | | Hole 3.0 MM Non-Plated | 1 | Hole-3.0mm_Non-Plated | | |

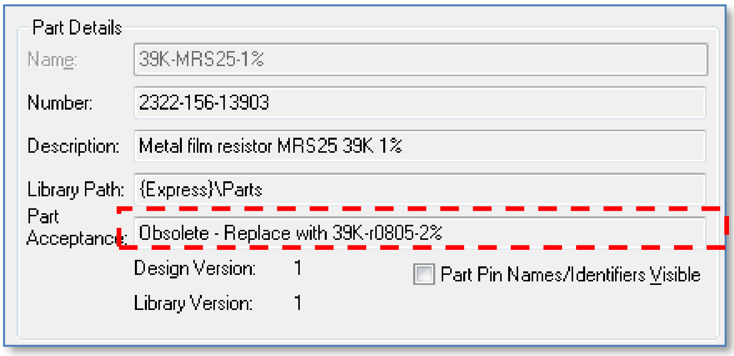
In the Parts Library image shown above, the column labelled "**Part Acceptance**" can hold a unique text reference to communicate a Part's Life cycle or inventory control measure to the user. This can be defined by the Librarian.

When a part containing a Part Acceptance value is added to a schematic design, the following warning dialog will be displayed.




Accepting this part will also store its value in the design for later reflection in parts List and various other report outputs.

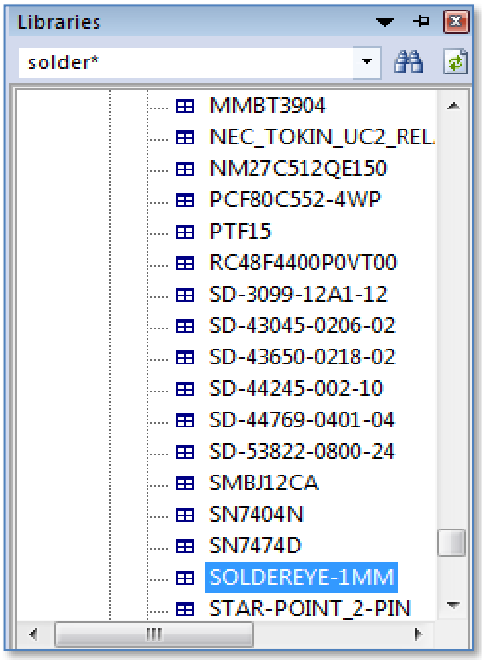
The property will be reflected in the Item Properties dialog.



8. After all the components have been placed, perform a Library search for SOLDEREYE-1MM. You can use the wildcard and search for solder*. You can then add these parts to represent the 8 Ohm Speaker, Input and +9V terminals (see schematic diagram on page 6). These parts will serve as the wire connections to the battery pack, signal input and speaker outputs.

   These parts are created as single pin **Testpoint** components. You could also add these by using the Add Testpoint command.

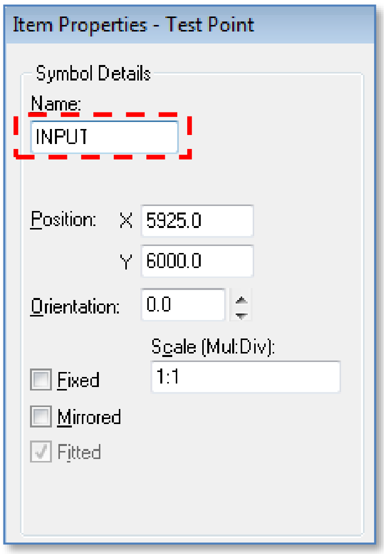
   Parts are assigned the next available Reference Designator per the design or the sheet. There are several ways to name or rename parts, such as with the Item Properties dialog.

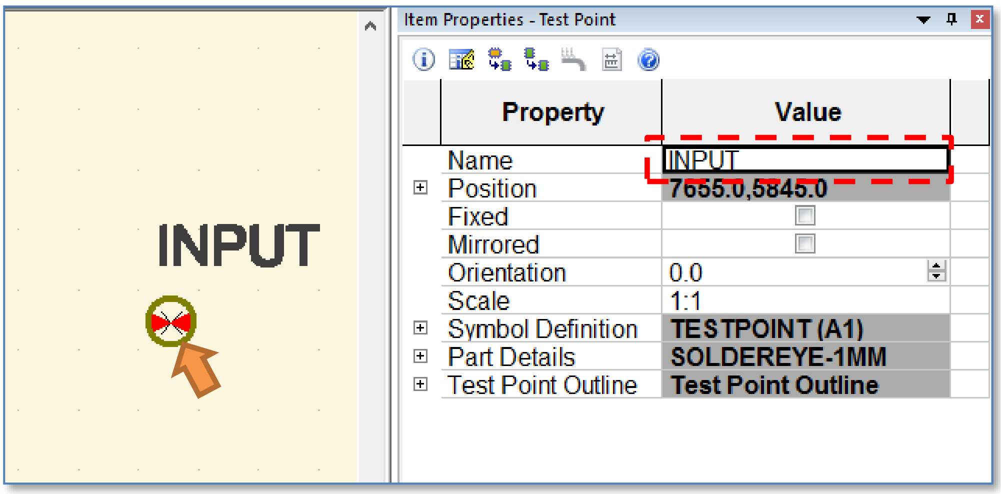



9. Change the Symbol Properties name for one of the SOLDEREYEs to "**INPUT**". To change the name, select one of the parts then click the <**R.M.B.**> and select **Item Properties**.

   Enter the corresponding name per the parts placement image on the previous sheet. Click the [**Close**] button and select the next Solder Eye part.

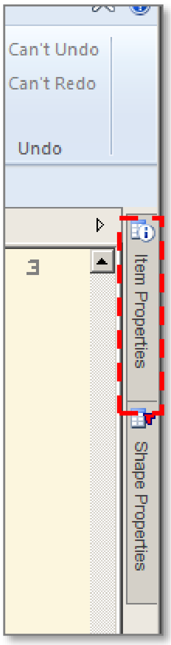
   You may repeat the same technique or use the ***non-modal*** **Item properties** auto-hide panel on the right side of the application window.

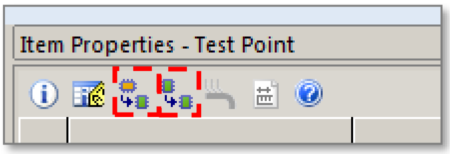


10. Pass the cursor over the *Item Properties* panel button to reveal the panel dialog. Set the pin icon to leave the auto-hide panel open for as long as necessary.

    With the panel open, the properties of any item selected will be represented. Many fields are editable. Functions such as Reload and Replace parts can be executed from the dialog. Other icons provide access to the standard *Item Properties* dialog and the *Attribute Editor*.

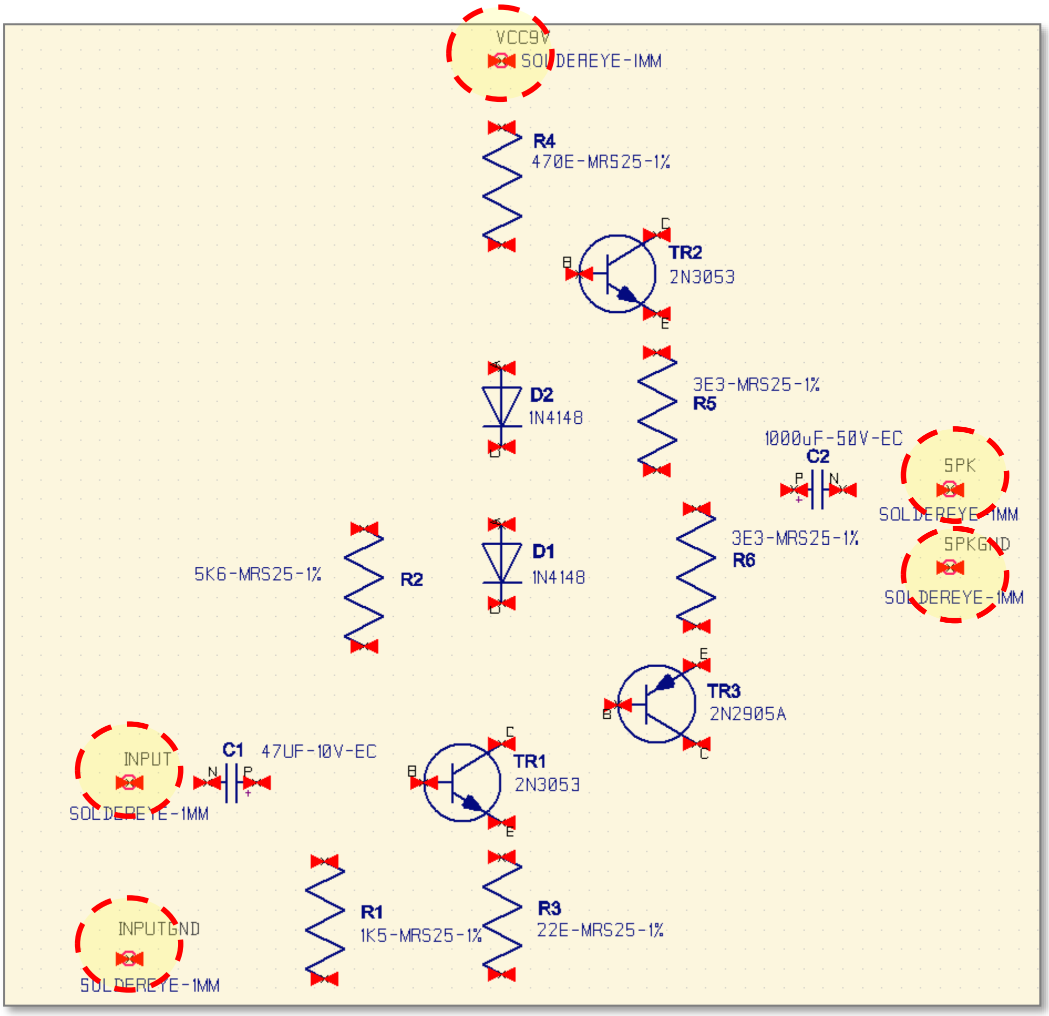



The spread sheet readability can be enhanced by clicking in the dialog to turn the Item properties title block blue then holding down the <Ctrl>key whilst using the **M**iddle **M**ouse **B**utton **<M.M.B.>** scroll wheel to adjust the magnification.

Use this option to name the SOLDEREYE parts according to the previous parts arrangement image. Simply select a part and enter its name one at a time. Since this is non-modal there is no need to close the dialog.

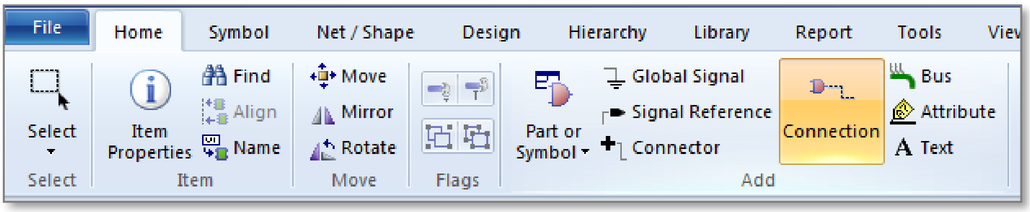
Place INPUT, INPUTGND, SPK, SPKGND, VCC9V as shown below.



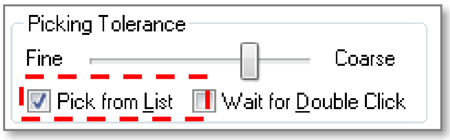
## Adding Connectivity

Adding connections can be achieved several ways.

a. Select the **Home** [tab] and click the **Add Connection** function. Click on a pin to start the connection, and move your cursor to your destination pin to complete the connection. The **Connection** function is also located on the **[Net/Shape]** tab.

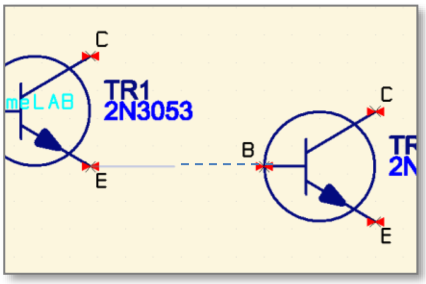


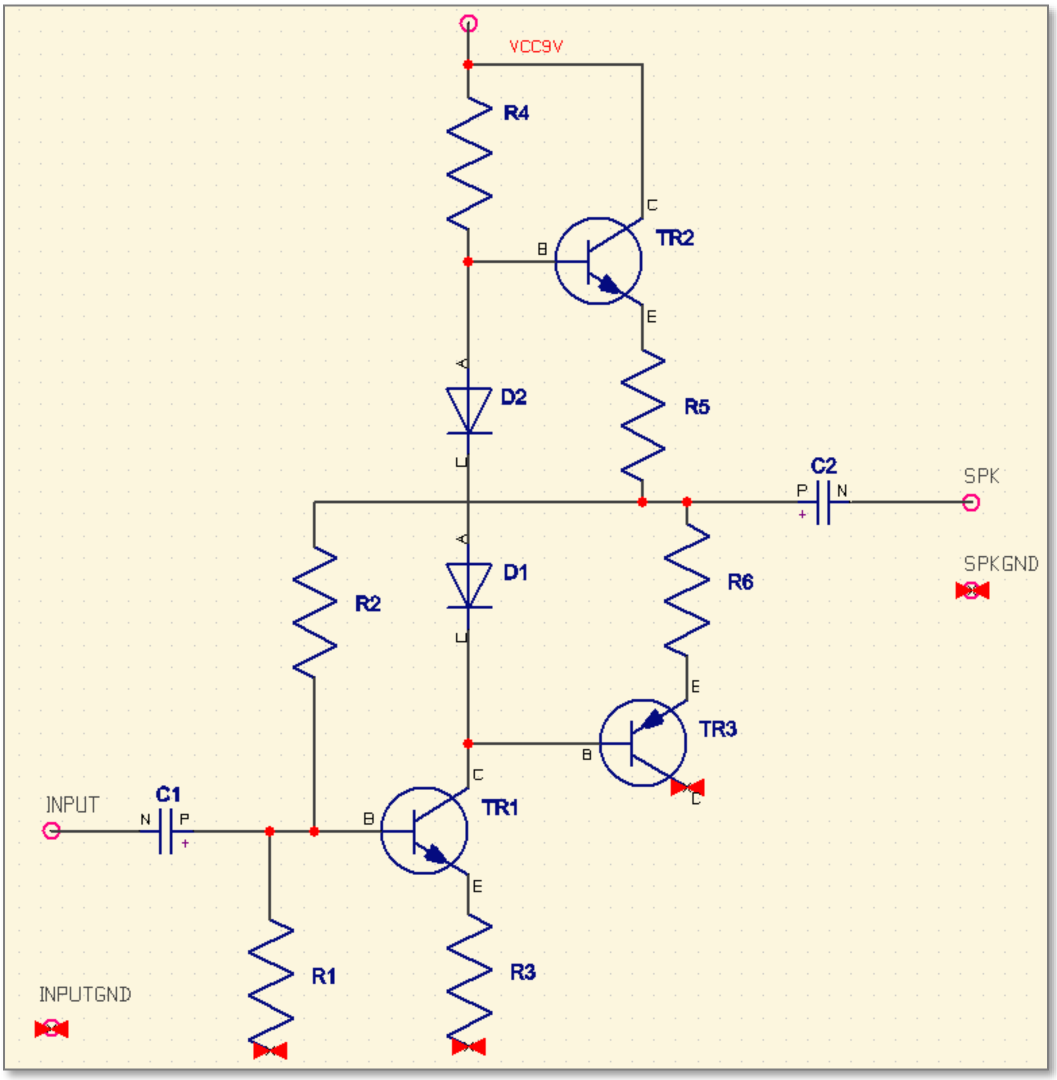

**Note:** By default, clicking on a pin will display a selection list. To disable this mode, select the **[File]** tab → **Options→[Interaction]** tab and uncheck the ***Pick from List*** setting. By disabling this, connections can be added in a non-modal method by double clicking on the pin.




b. You can place the connecting terminals (pins) on top of each other, then drag them apart to see the connection. Pins that are connected will be automatically hidden.

c. You can use the left mouse button <**L.M.B.**> to click (hold and drag momentarily) from the red bow ties displayed on unconnected pins and click the left mouse button over another red bow tie to finish. Corners can be added along the way by also clicking the <**L.M.B.**>.

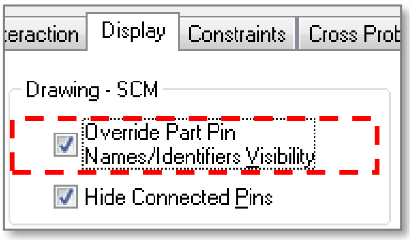





CADSTAR allows you to make pin names or numbers visible/invisible (this is typically determined by the librarian) such as for 2 pin non-polarized devices. If these parts are set to be invisible the user can override them globally as follows.

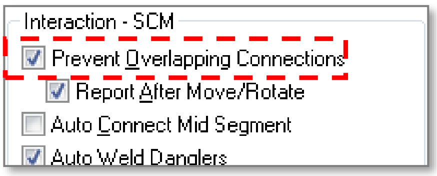
11. Select **[File]**tab→**Options**→**[Display]** from the ribbon and enable/disable **Override Part Pin Names/identifiers Visibility**.

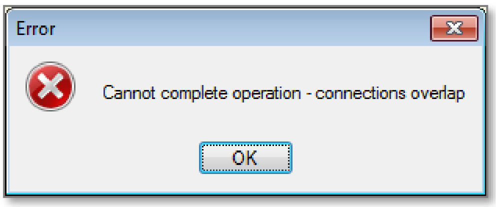
    CADSTAR provides an Interactive check for flagging overlapping connections.



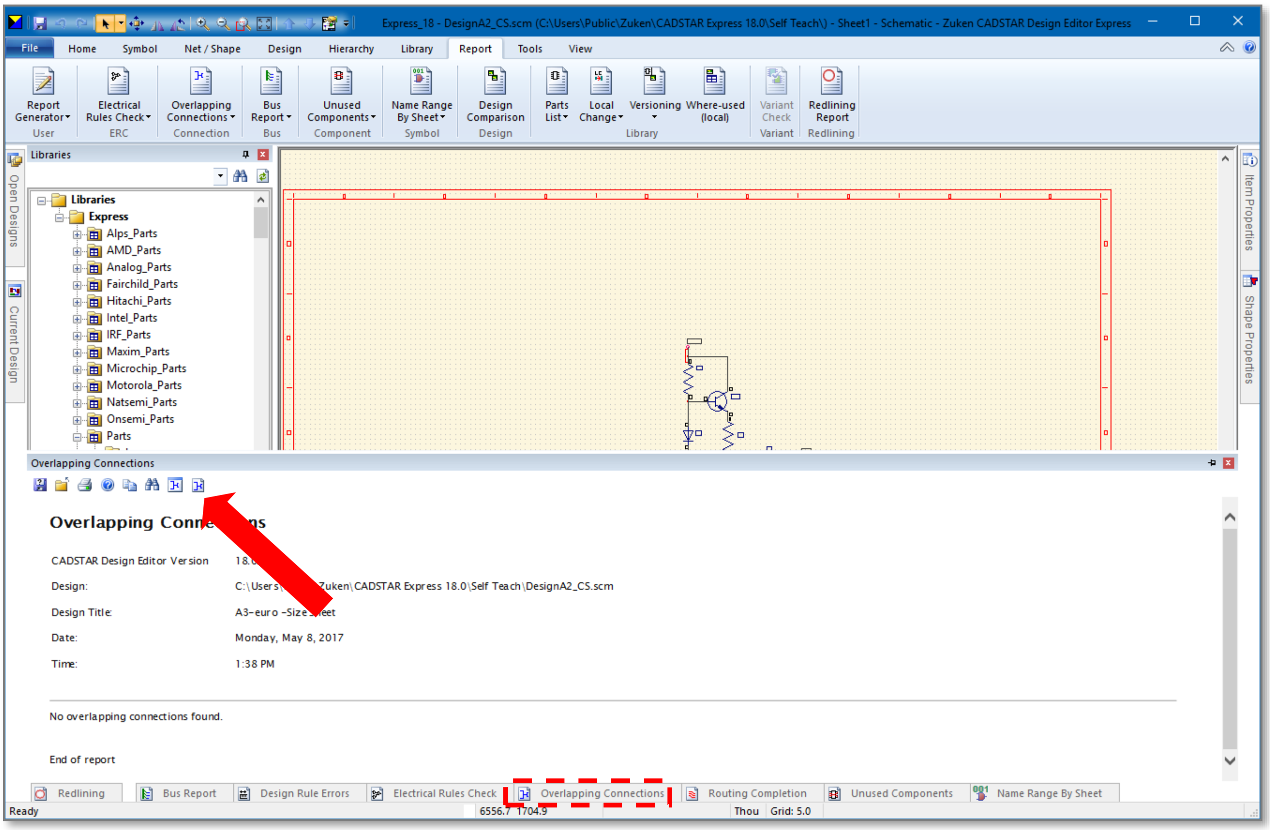

12. Select the [**File]**→**Options**→**[Interaction]**.

    When the **Prevent Overlapping Connections selection** is enabled, the check will alert you with the following error when you attempt to drag a connected terminal of any sort and place it on top of a connection line of a different net name.

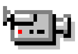


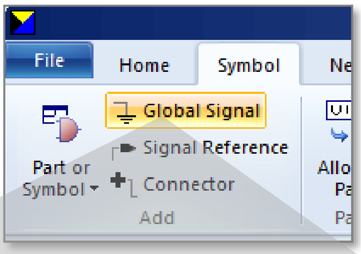
If you do not wish to run the interactive check until a more convenient time, simply disable the selection. When you are ready to perform a batch check of the design, move the cursor over the Overlapping Connection active report button to make the report panel open.



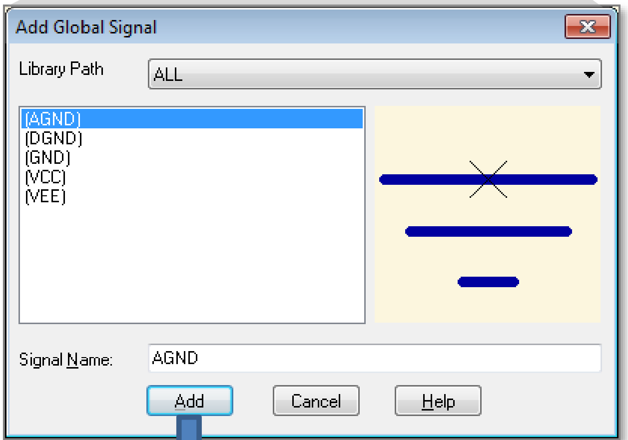

Click the **Overlapping Connection** report button as shown above. The resulting report contents are hypertext. Selecting a line item will make the error appear in the schematic window.

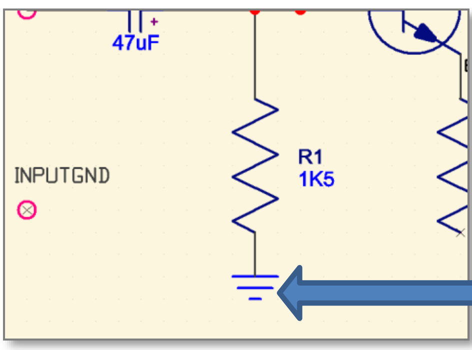


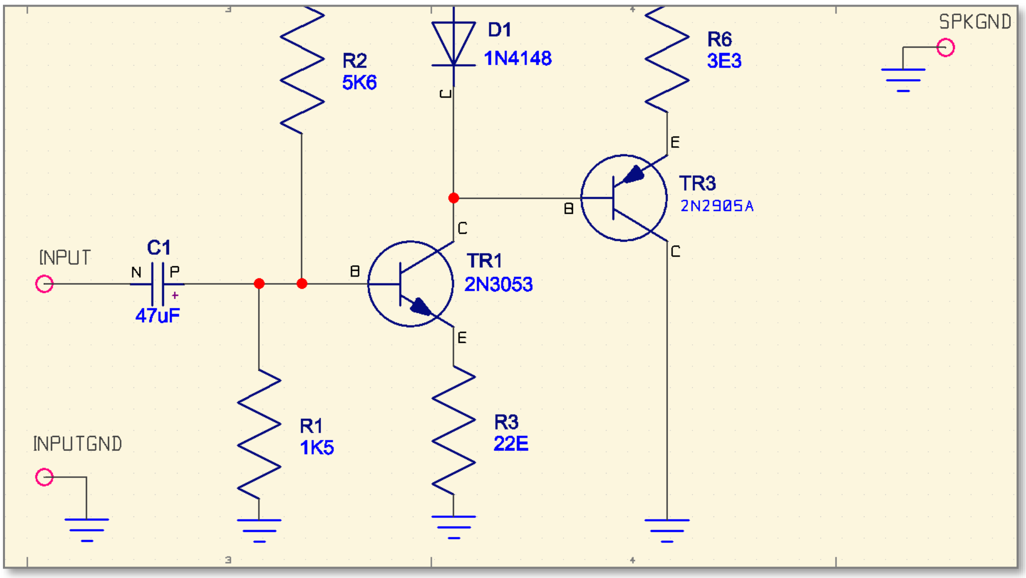
13. Add five AGND Global Signal symbols as shown in the diagram. To do so, click the **Global Signal** button located on the Symbol tab.




Select (AGND). You can connect the AGND terminal and the terminal of resistor R1 by placing the terminals onto each other as shown below.

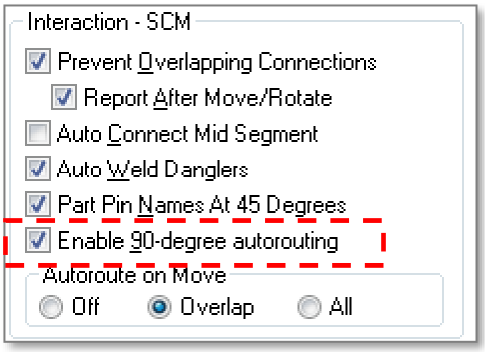





14. Finish connecting all the symbols together as shown on the previous page. To connect, try each of the methods as previously described.

    When you are adding a connection (**Add Connection**) or editing a connection (**Add/Edit Segment**) the route taken by the connection will automatically avoid obstacles in its path. This can be enabled/disabled in the **[File]→Options→[Interaction]**.



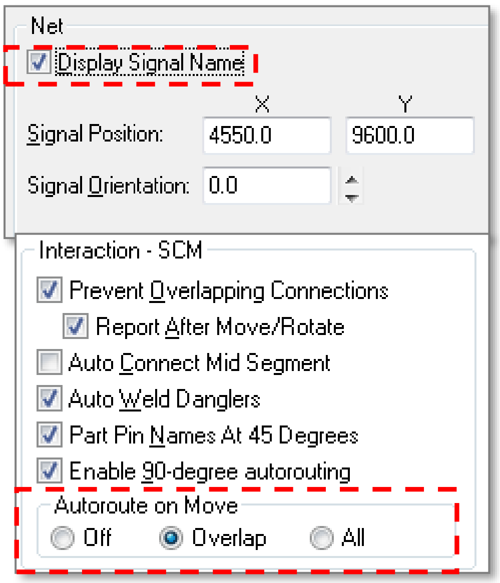

    When connecting, you can also use the right-hand mouse button <**R.M.B.**> to **Change Default Net Route Code**, allowing you to select a different Net-Route Code for the PCB design. (I.e. wider than signal tracks for Power & GND).

15. Change the net name connected to VCC9V to VCC by selecting the net and clicking the Item Properties icon.

16. Select the pins of the AGND symbols and click the Item Properties icon. Check the **Display Signal Name** option to display the AGND signal names.

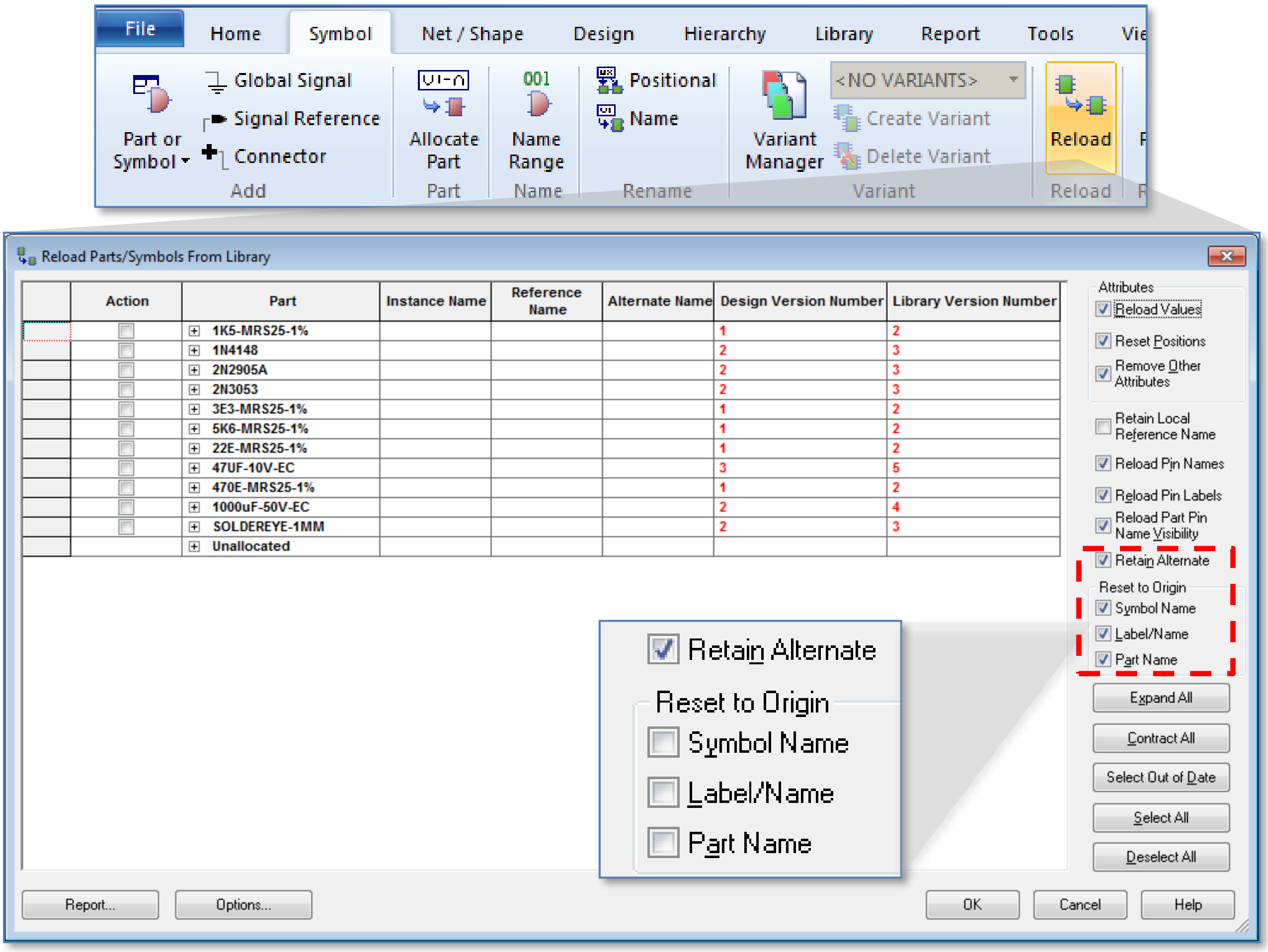
    **Note:** this is for display purposes only. If you decide to not show the signal names they would still remain AGND.

    **Note:** Moving connected symbols maintains connectivity as you would expect. A connection autorouter corrects the 90 degree orthogonal patterns in real time. However this can be disabled if you wish.



If **Automatic Version Increment** in **[File]→*Options*→[System]** is enabled, with every future change of a symbol, component and part, the version increments automatically as it is saved to the library. You can easily check if a component in your Schematic or PCB design matches the current Library version. To check, click **Reload** located on the **Symbols** tab.

This function is also used to reset all selected parts, Label, Symbol and Part name attributes to their original locations as defined in the library by selecting a ***Reset to Origin*** option.



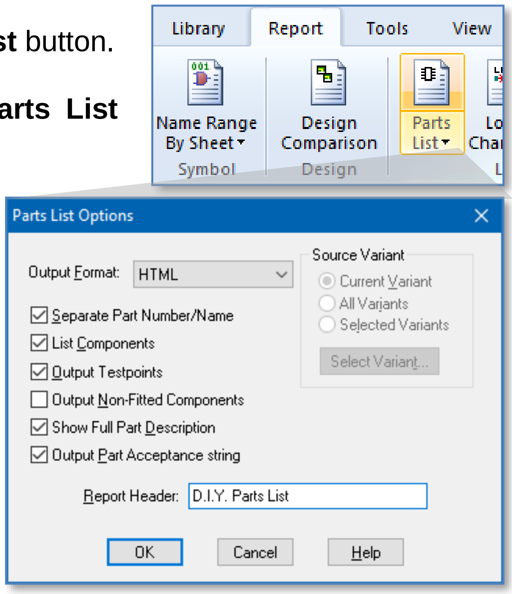

The image The image shown above is an example that shows the dialog when Parts are different than those in the Parts Library.

17. When completed, save this schematic design as **DesignA2.scm.** If you didn't complete the schematic design as described above, just open DesignA2_CS.SCM and save it to overwrite your file.

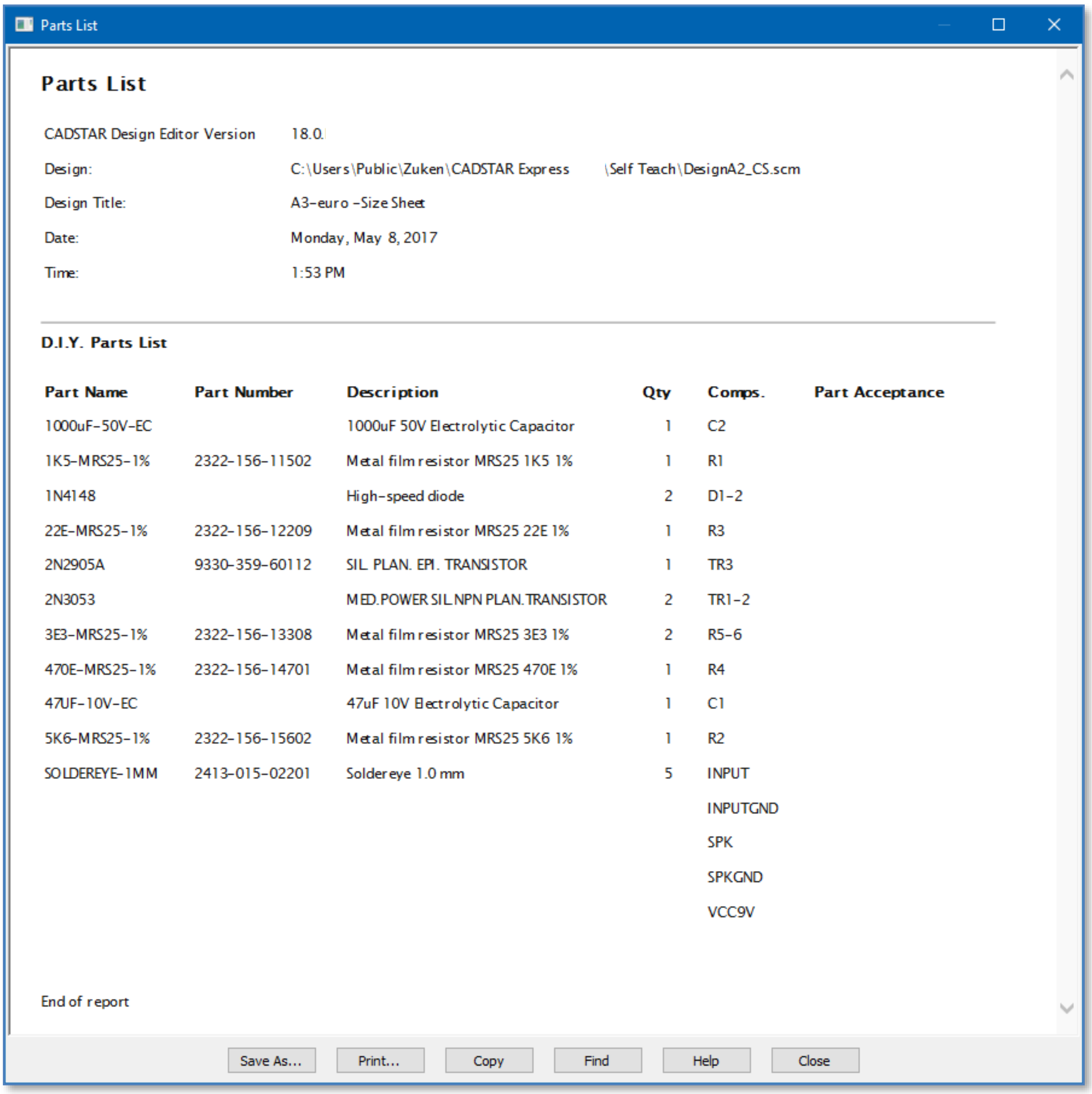
18. In today's market it is important to deliver a B.O.M. (Bill of Materials or in CADSTAR called Parts List) at an early stage.

To create a parts list, click the upper half of the **Parts List** button.

To modify the options select the lower half of the **Parts List** button.




The output shown below includes the Parts description and the Testpoint components.



Parts List

## Parts List

| | |
|---|---|
| CADSTAR Design Editor Version | 18.0. |
| Design: | C:\Users\Public\Zuken\CADSTAR Express \Self Teach\DesignA2_CS.scm |
| Design Title: | A3-euro -Size Sheet |
| Date: | Monday, May 8, 2017 |
| Time: | 1:53 PM |

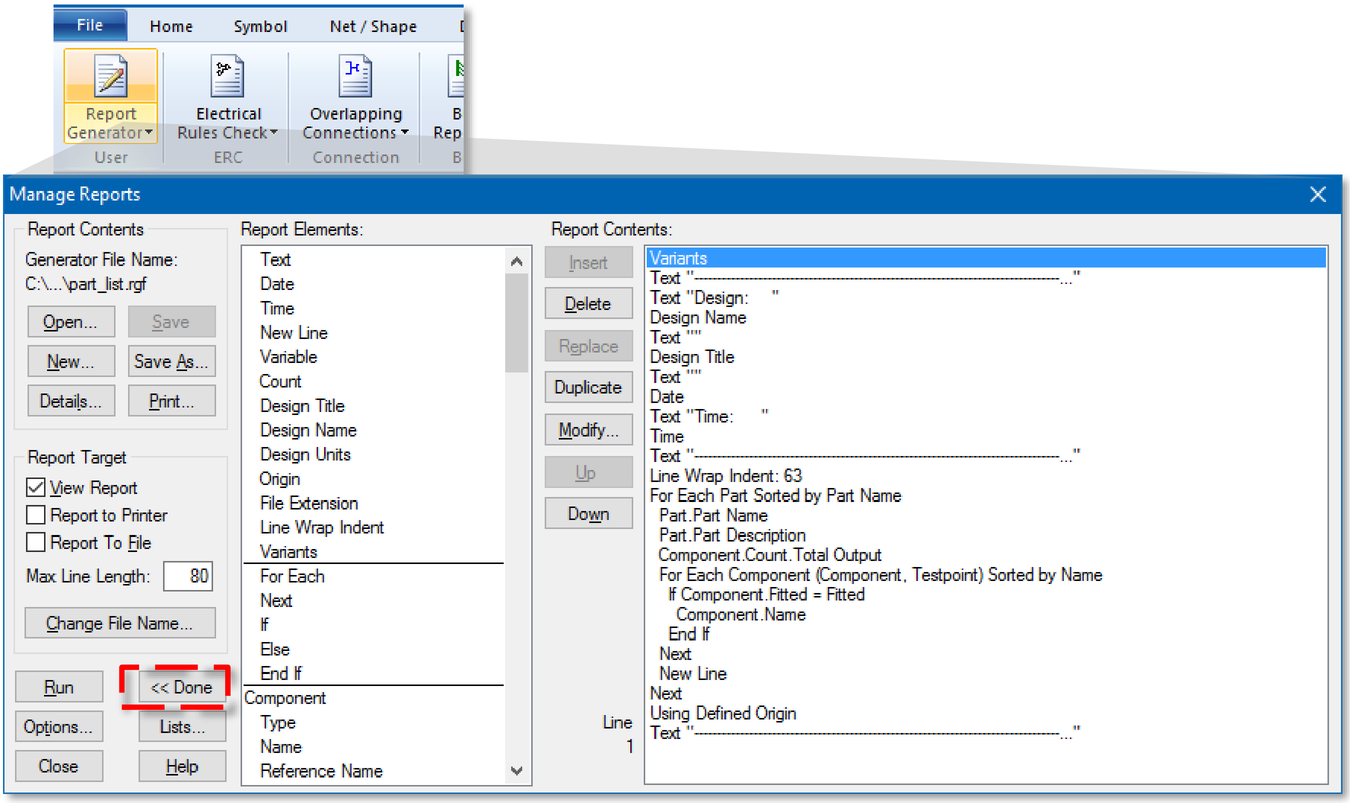
**D.I.Y. Parts List**

| Part Name | Part Number | Description | Qty | Comps. | Part Acceptance |
|---|---|---|---|---|---|
| 1000uF-50V-EC | | 1000uF 50V Electrolytic Capacitor | 1 | C2 | |
| 1K5-MRS25-1% | 2322-156-11502 | Metal film resistor MRS25 1K5 1% | 1 | R1 | |
| 1N4148 | | High-speed diode | 2 | D1-2 | |
| 22E-MRS25-1% | 2322-156-12209 | Metal film resistor MRS25 22E 1% | 1 | R3 | |
| 2N2905A | 9330-359-60112 | SIL PLAN. EPI. TRANSISTOR | 1 | TR3 | |
| 2N3053 | | MED.POWER SIL.NPN PLAN.TRANSISTOR | 2 | TR1-2 | |
| 3E3-MRS25-1% | 2322-156-13308 | Metal film resistor MRS25 3E3 1% | 2 | R5-6 | |
| 470E-MRS25-1% | 2322-156-14701 | Metal film resistor MRS25 470E 1% | 1 | R4 | |
| 47UF-10V-EC | | 47uF 10V Electrolytic Capacitor | 1 | C1 | |
| 5K6-MRS25-1% | 2322-156-15602 | Metal film resistor MRS25 5K6 1% | 1 | R2 | |
| SOLDEREYE-1MM | 2413-015-02201 | Soldereye 1.0 mm | 5 | INPUT | |
| | | | | INPUTGND | |
| | | | | SPK | |
| | | | | SPKGND | |
| | | | | VCC9V | |

End of report

Save As... Print... Copy Find Help Close

If you prefer to create a Parts List in a different format (fully customizable) click on the **Report Generator** button also located on the **Reports** tab.




In the above image the dialog is fully enlarged as a result of clicking the [**EDIT**] button.
Once enlarged the button will change to [**Done**] thus serving as a toggle function.

Open the file ***part_list.rgf***, which you can find in the *Reports* directory and just click [**Run]**. You can customize the parts List output and list any attribute (wattage, voltage, tolerance, manufacturer etc.) in any particular order you choose.

For the more advanced users among you who have experience in Visual Basic or C++, you can create, for example, a user-defined B.O.M in Microsoft Office Excel, by using the OLE automation in CADSTAR.

19. To print your schematic design, simply click on **[File]→Print** and go through the Print and Page Setup. Alternatively you can print your schematic design to a PDF file, you do not need to install a PDF writer, CADSTAR has its own native PDF writer.

**Tip:** *Enable Alternative text output* in the print options, making text ***searchable*** when printing to a file format such as ***PDF***.

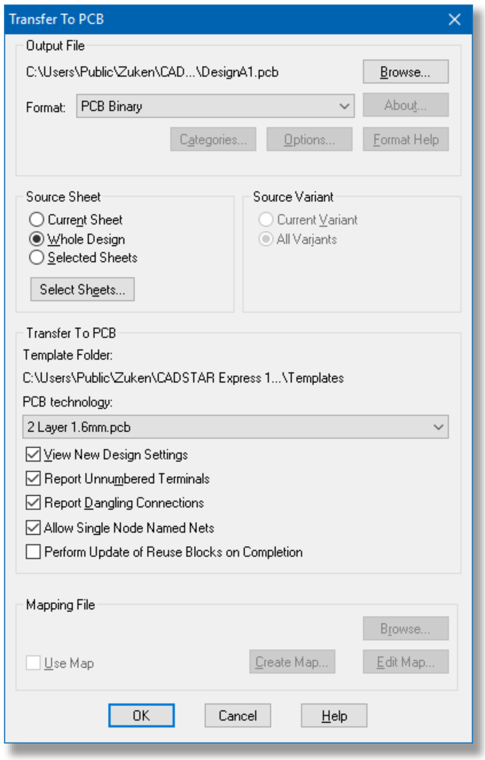
CADSTAR

20. Finally, transfer the schematic to PCB through **[Design]→Transfer to PCB**.

The dialog will automatically use the same *output file* name as the schematic being transferred. Click the [**Browse**] button to enter a different name.

Set the output file to **DesignA1.pcb** as shown →

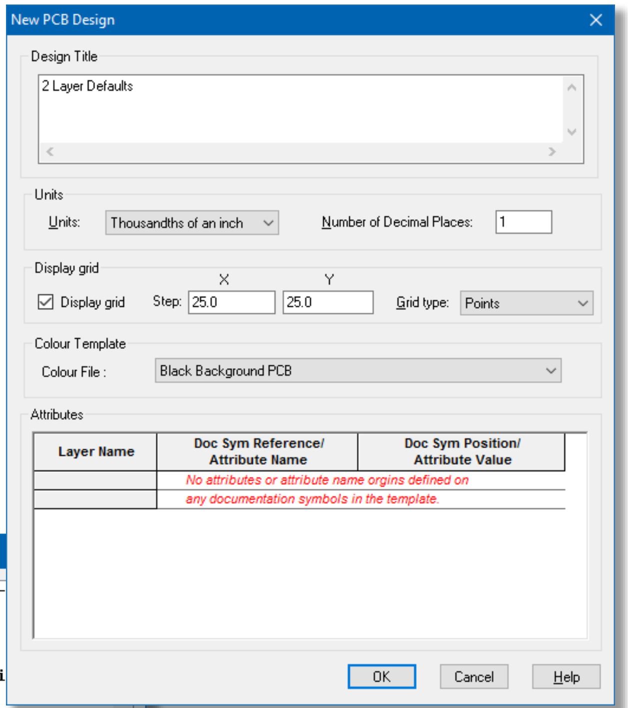
Choose **'2 layer 1.6mm.pcb**' as PCB Technology. Click [**OK**]

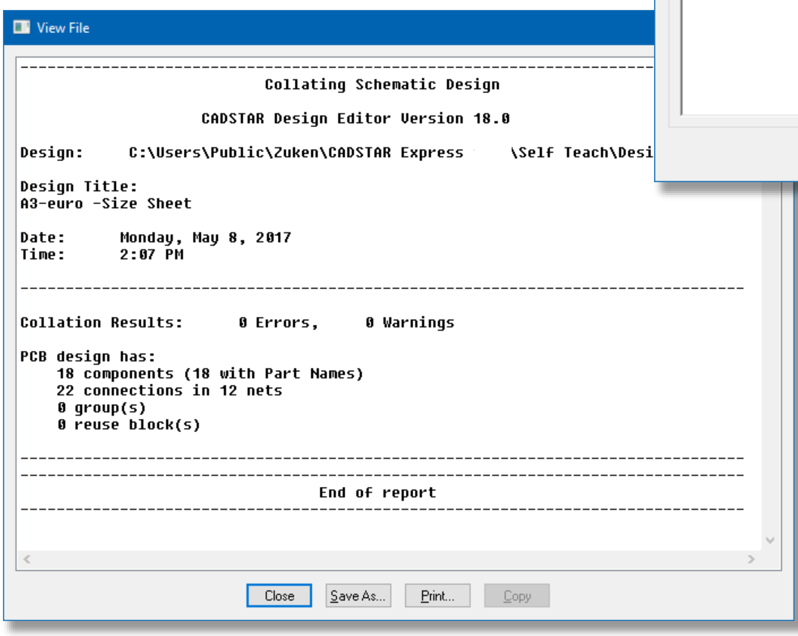



As part of the process a report is generated identifying any warnings or errors that may be in the Schematic design.

Next specify the PCB design units, Display Grid dimensions, default colour template and enter any initial attribute values if required by your company PCB technology templates.

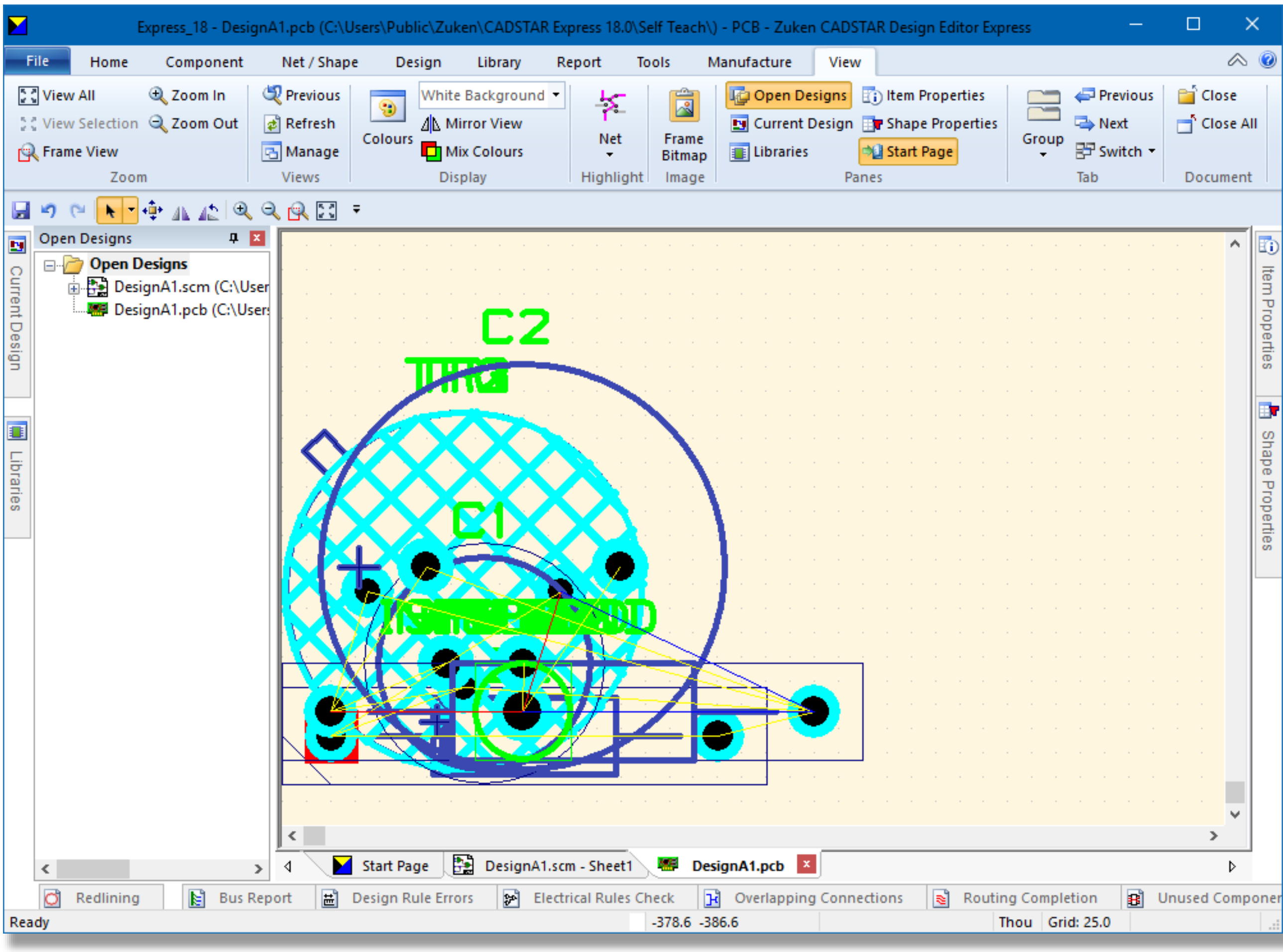
Once the schematic data is collated error free, you will be prompted with the adjacent dialog. Click [**Close**]

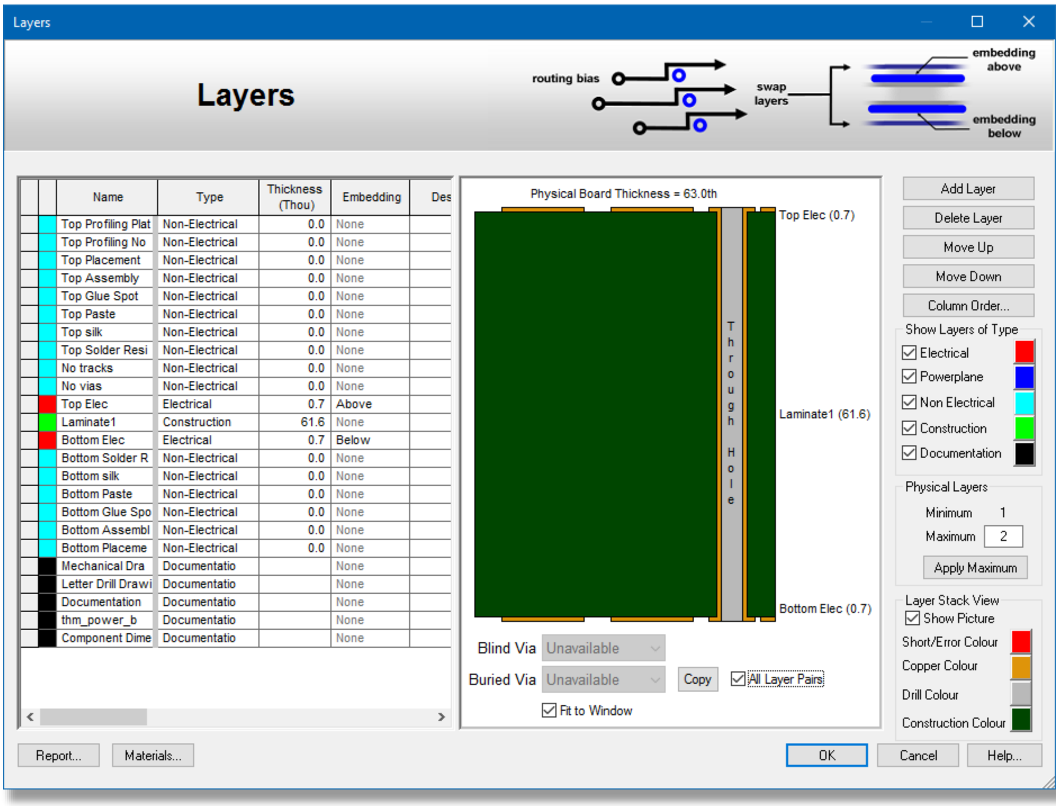



← Click **[Close].**

The PCB Design will appear in a new window, active with a PCB related ribbon style GUI.




***Note:*** If you choose the PCB Technology **'1 layer 1.6mm.pcb'** during transfer to PCB, this default technology file is prepared for single sided boards. The advantage of the different technology files is that you still can make use of ONE library as you will experience in Design D.

The first steps showed how a schematic design can be drawn for Design A.  In fact, any schematic can be drawn following the sequence shown. However, a more complicated design will require more challenging steps. There are many tools within CADSTAR Design Editor that will help designers like you to create a schematic. You can also add spacing classes, insert a component into a net without any disconnection, and perform auto-connection of busses. Other tools like Align Symbol, Design Re-use, Design Variant, Hierarchical Design, etc. are also important and are user friendly for professional design engineers to use.

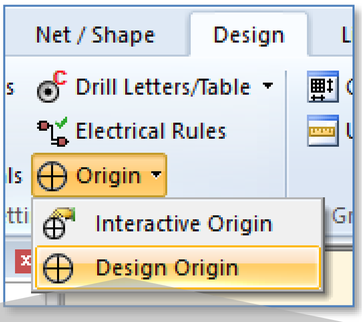
You can now move on to PCB Design. You will notice that the CADSTAR Library, Schematic and PCB design editor run on the same Graphical User Interface, guaranteeing a fast and problem free transfer.

## Step 2 - PCB Placement for Design A

If you didn't create the new PCB design as described, just open **DesignA1_CS.PCB** and save it as **DesignA1.PCB**

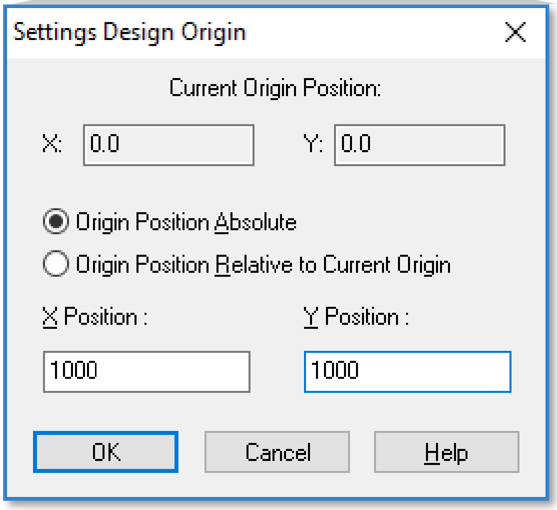
1. Set the design units to "Thou" (Thousandth of an Inch) by selecting **[Design]→Units** or alternatively by double-clicking the units Thou Grid: 5.0 at the bottom of the CADSTAR window.

When a new PCB design is created all components are placed in the positive quadrant of 0X, 0Y, this is considered the initial Design origin.




2. Select the [**Design**] tab and click on [Origin → Design Origin].

   You will see the design origin symbol at 1000 for both X and Y position. This is defined in the **'2 layer 1.6mm.pcb**' PCB Template that was used.




Next, you will have to create a PCB outline;

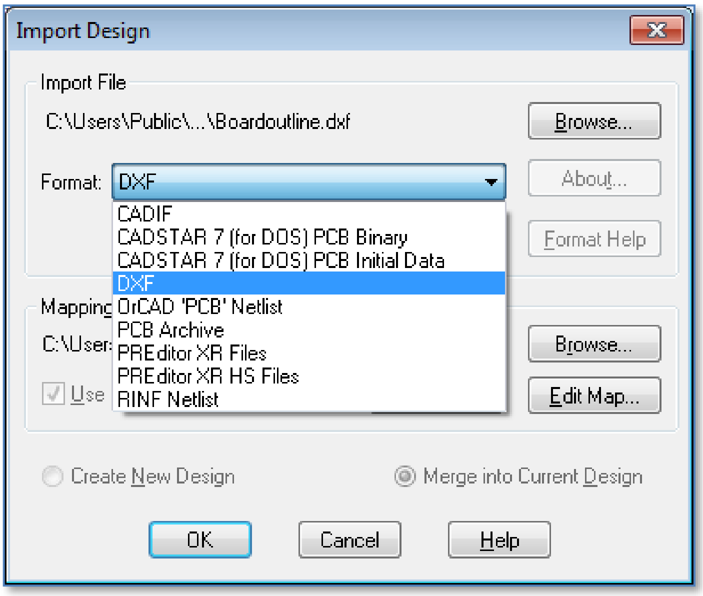
A board outline can either be created within CADSTAR or imported via DXF format.

**3.** Select **[File]** tab→**File Import**. **Change the Format to DXF.**

Select the DXF file ***Boardoutline.dxf***.

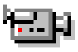
For the Mapping-file, you have to select **dxfin.map**, which you can find in the ***../user/*** folder and just click [**OK**].

If you have chosen to import the DXF board outline, then skip to step 7.

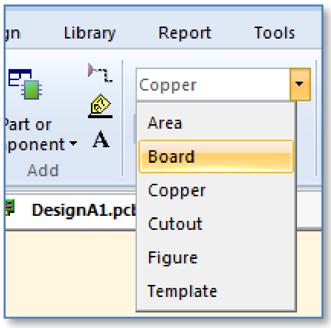


**Note:** the board outline that is imported using the DXF data is different from what is described in step 4. The intent is to demonstrate the support for DXF Line entity styles such as BLOCK, INSERT, ELLIPSE, SPLINE and POLYLINEs.

CADSTAR also supports Importing and Exporting of IDF 2.0 and 3.0 from most mechanical CAD systems.



4. Alternatively you can manually draw the board outline.



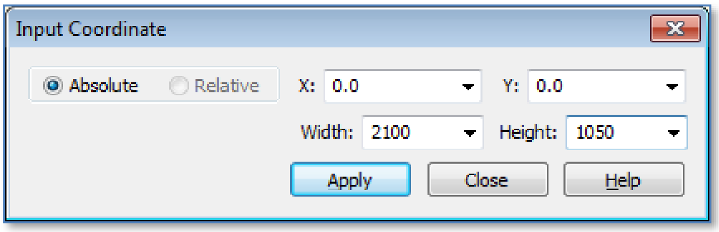

Let's try to do this by inputting coordinates using a dialog.
Locate the ***default shape type*** *quick-pick* menu on the **[Home]** tab and change the default to **Board** as shown to the right. →
Next, click the "Add Rectangle" button.

Click the <**R.M.B.**> and select **Input Coordinates.**

Enter a Width value of 2100.
Enter a Height value of 1050.

Leave the other fields as shown →

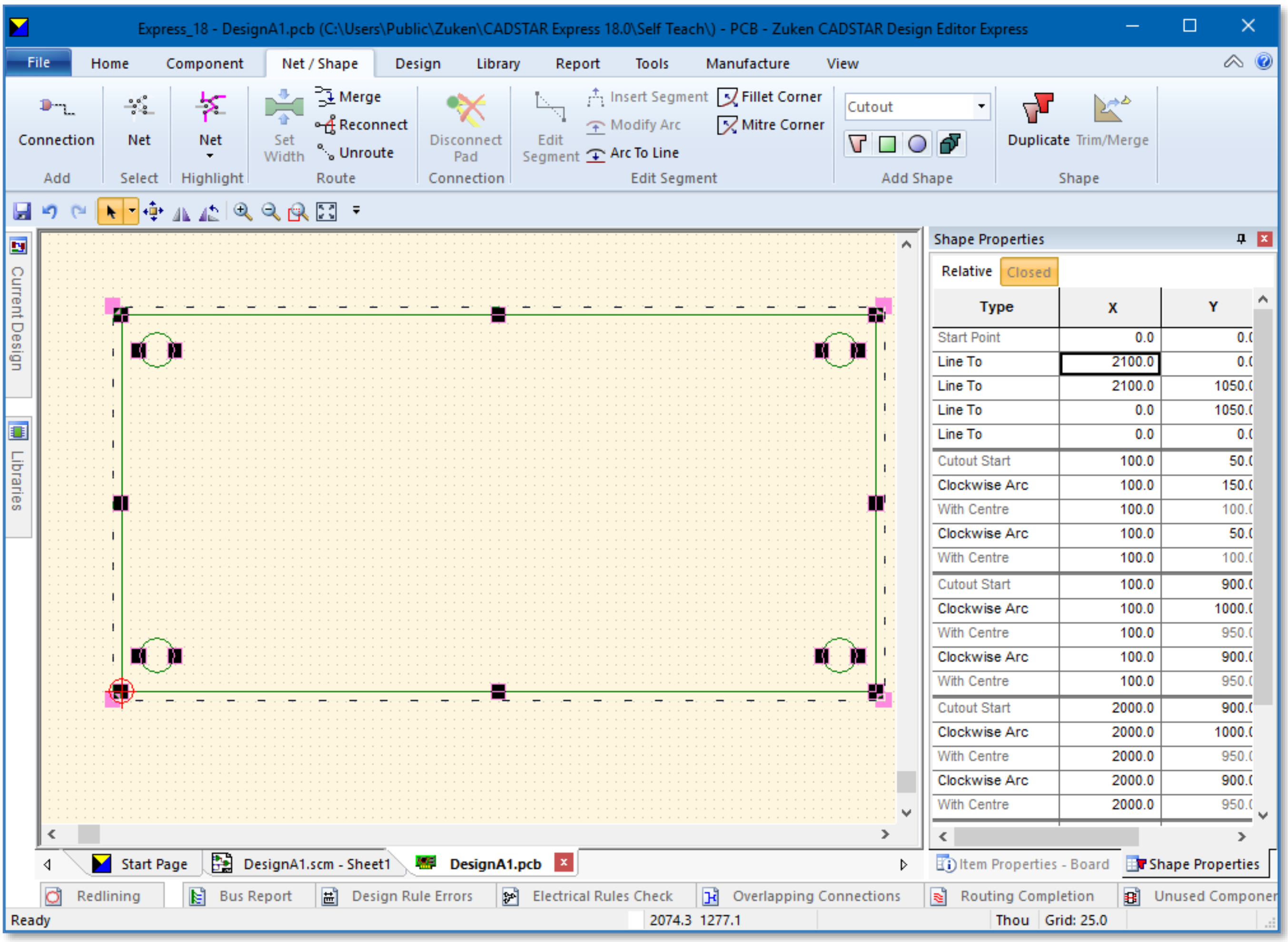
Click [**Apply**]




**Note:** if you choose to create the shape without the use of the ***Input coordinates*** assistant watch the absolute and incremental coordinates at the bottom of the CADSTAR window when drawing the board outline.

**Tip:** From any point in the design you can reset the incremental coordinates by pressing the 'Z' key, followed by the <**Enter**> key.

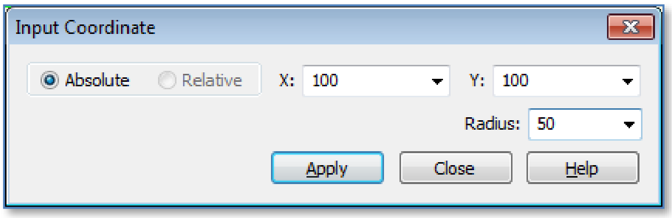
5. To modify any outline (board, figures, component outlines etc.), simply click on the shape edge and select one of the grab handles. You can also use the Shape Properties panel on the right side of the application window. By selecting the outline you can see and modify the absolute or relative coordinates.




6. You can also create screw holes or mounting holes if you like. To do this within the board outline locate the ***default shape type*** quick-pick menu and change the default to **Cutout**, and then click any of the drawing tool icons . In this case you will add four round holes with a 50 thou radius.

   Click the **Add Circle** icon.

   Click on the board outline then click the <**R.M.B**.> to select the **Input coordinates** assistant.




   Enter X 100 Y 100 as the location of the center of the cut-out and enter a Radius of 50 thou.

   Click [**Apply**]. The Input coordinates assistant will remain open.

   Remember to select the board outline before selecting each add shape as per the command line instructions.

   If the board outline is in full view you should see the first cut-out in the lower left corner of the rectangle.

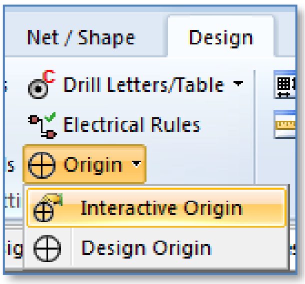
   Add cut-out number two at X 100 Y 950.

Retrieve the previous radius value of 50 from the pull down list and click [**Apply**]. The Input coordinates assistant will remain open.

Repeat the sequence for cut-out number three at X 2000  Y 950 and cut-out number four at  X 2000 Y 100.

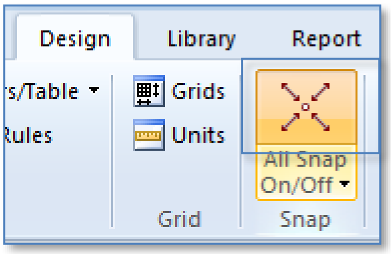
If you didn't manage to draw the board outline or to import the board outline through DXF, just open **DesignA2_CS.pcb** and save it as **DesignA2.pcb**. Note the board shape is as shown above.

Once the board outline has been imported or drawn manually you can set an interactive origin, to reference all X and Y co-ordinates of all design items, and cursor positions, relative to the new origin.




7. Select **Interactive Origin** from the **[Design**] tab and place the origin at the lower left corner of the board.

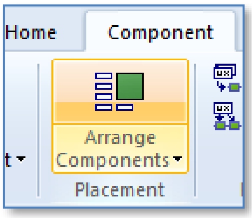
Enable Snap to Endpoint it will be even easier to place the Interactive Origin. To do so select **All Snap on/off** located on the **[Design]** tab.



## Component Placement

Start by moving or arranging the components around the outside of the board outline.

8. Use the Arrange Components function, located on the [**Component**] tab to move the components from zero, zero.

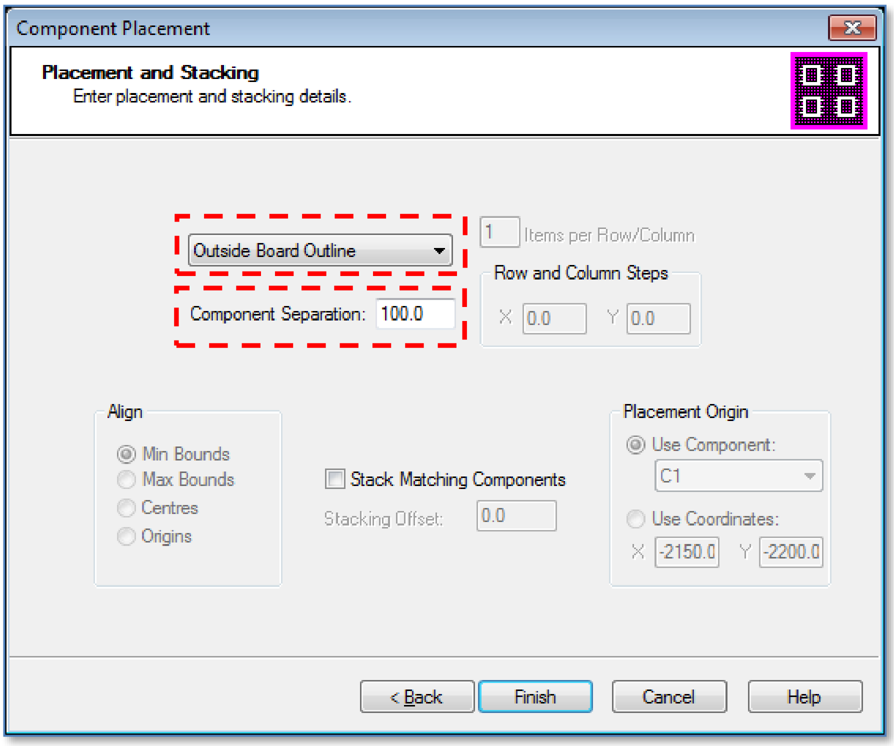



Select the ***Place around board outline*** option on the first dialog and click **[Next]..**

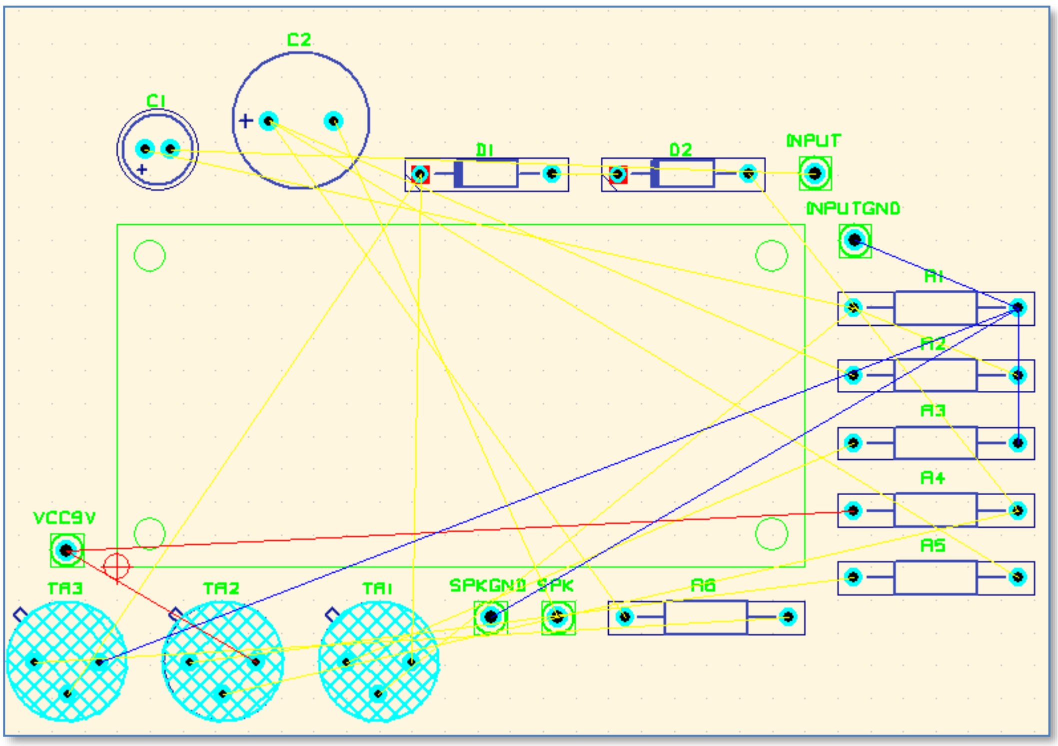
Set the method to **Outside Board Outline.**

Set the **Component Separation** to **100.**

Click **[Finish]**




Your results may vary.



Place the critical components inside the board outline. In this sample design, the SOLDEREYE parts should be placed first. You may consider these components as critical where as their location would be described by mechanical engineers. This is also possible in CADSTAR using the BoardModeler Lite application as well as the IDF Module If you do not have BoardModeler Lite or the IDF Module. You can use the ***Item Properties*** panel to enter placement criteria such as X, Y Coordinates, Rotation and Board side.

**Note:** BoardModeler Lite and the IDF Module are available for evaluation by contacting your local CADSTAR Sales Agent.

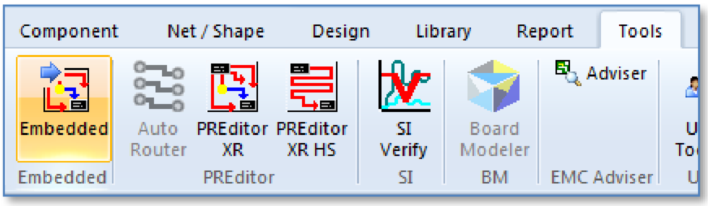
9. Open the non-modal *Item Properties* panel located on the right side edge of the application window. Click the pin icon for it to remain open.

10. Select component VCC9V by clicking on the outline or just type in “VCC9V<Enter>”. (It will be highlighted automatically), then change the X-position to 250,0 and Y-position to 875,0 and click the **Fixed** tick box.. The component will move to the new location. Click in the PCB window.

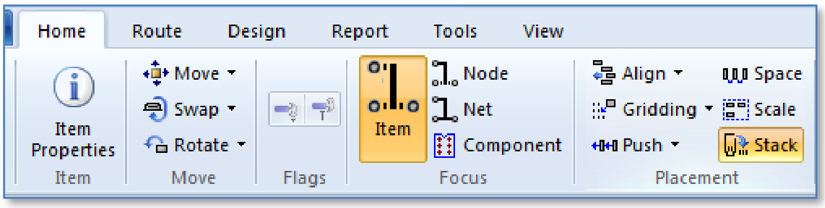
    Repeat this action for:

    Component SPKGND, change the X-position to 450.0 and Y-position to 875.0
    Component SPK, change the X-position to 650.0 and Y-position to 875.0
    Component INPUT, change the X-position to 1650.0 and Y-position to 100.0
    Component INPUTGND, change the X-position to 1850.0 and Y-position to 100.0

11. Place the remaining components by selecting the Embedded Place and Route icon located on the [**Tools**] tab.

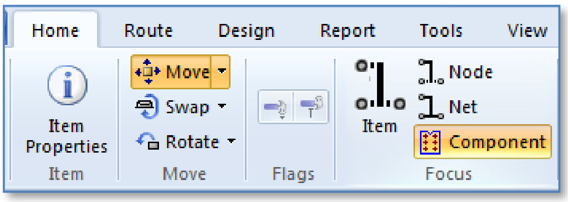



Select the **[Home]→Stack off-Board** icon.

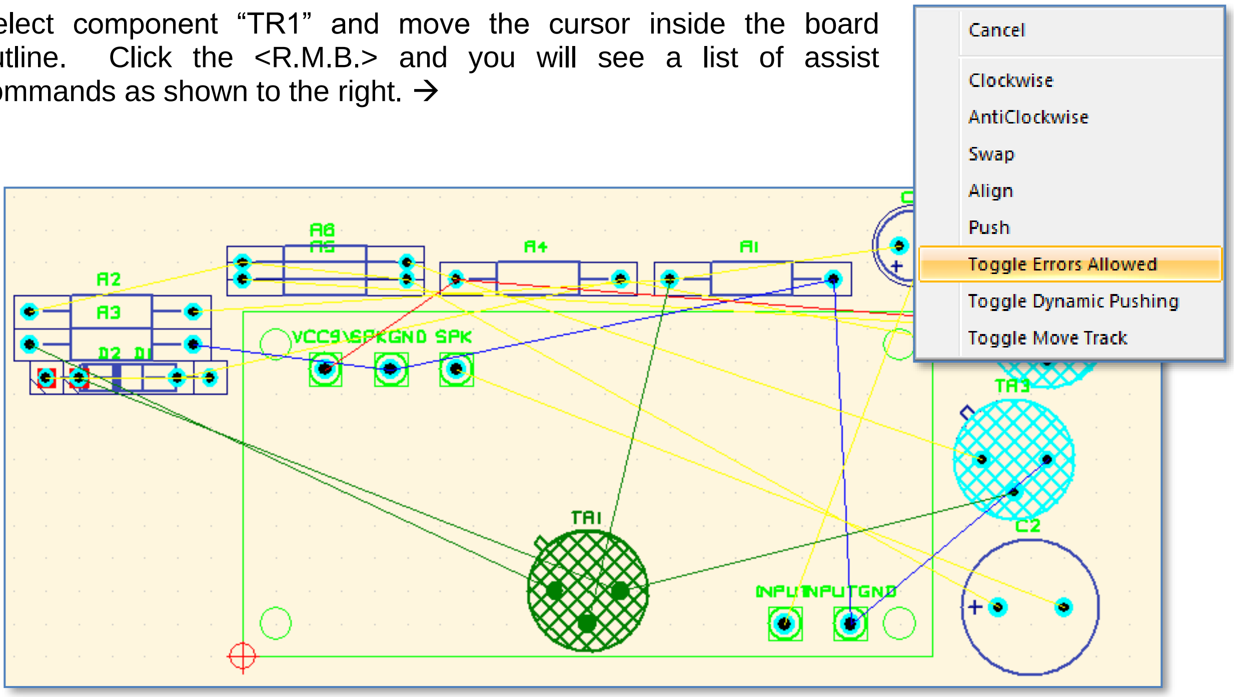



Enter <**Ctrl+A**> to select all components. This will result in all the components that are currently unfixed to be randomly placed around the perimeter of the outline. This serves as a second option for arranging components.

12. Select the **Move** icon and the **Component** mode focus icon.



13. Select component “TR1” and move the cursor inside the board outline. Click the <R.M.B.> and you will see a list of assist commands as shown to the right. →



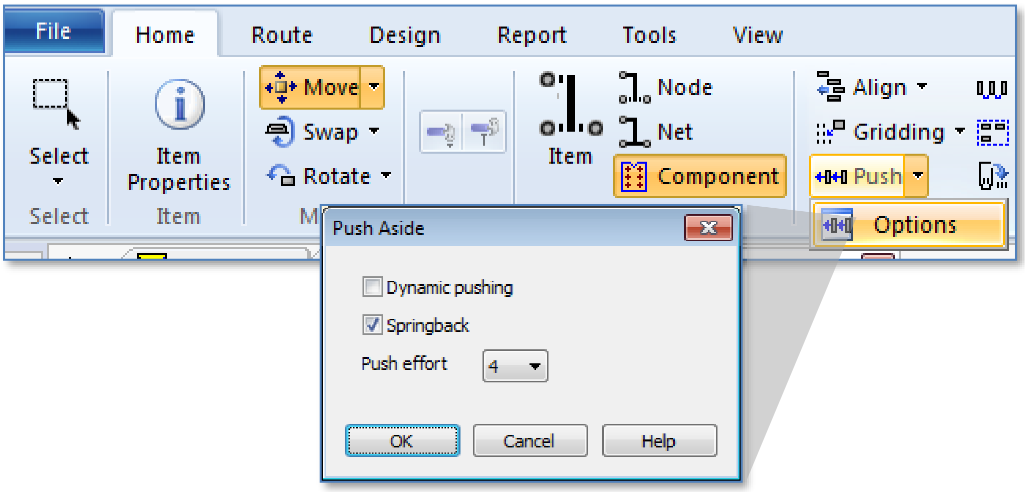

Selecting **Clockwise** or **Anti-Clockwise** will rotate the component accordingly. You can do so by pressing ‘**C**’ or ‘**A**’ on the keyboard to gain the same result.

Selecting **Swap** will mirror the component shape to the opposite placement side.

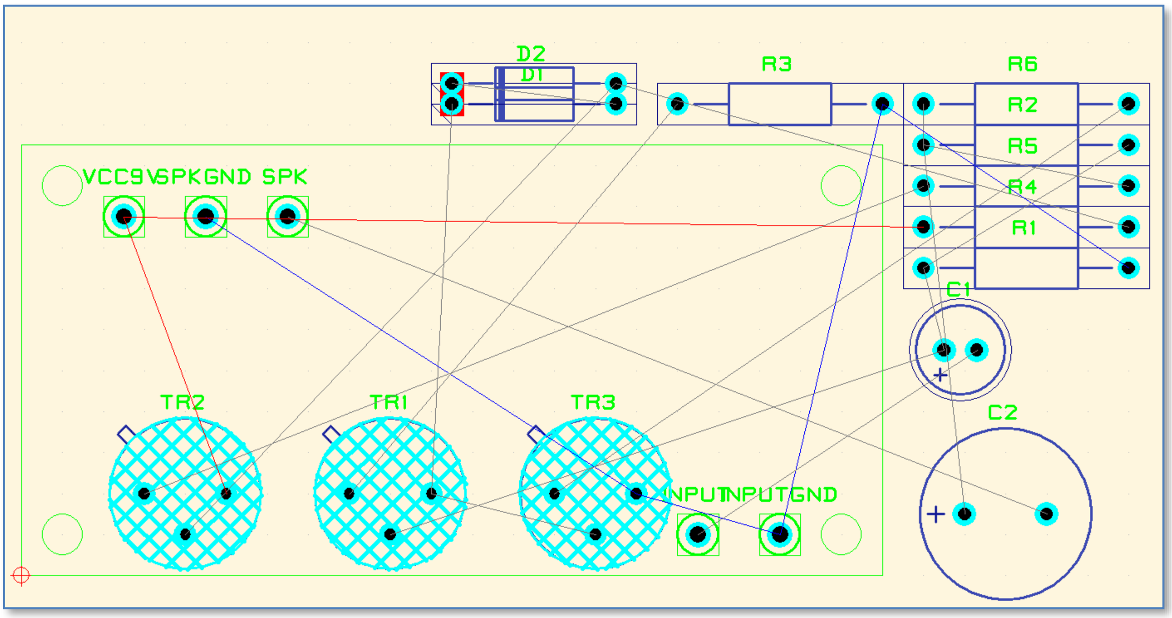
The Embedded Placement tool will aid in error free placement. However, there are times when an error is needed temporarily. Such as, to place a component back outside of the board outline temporarily. This can be achieved by selecting "**Toggle Errors Allowed**".

If the default action is to push other components, the opposite behaviour can be chosen using the **Toggle Dynamic Pushing**.

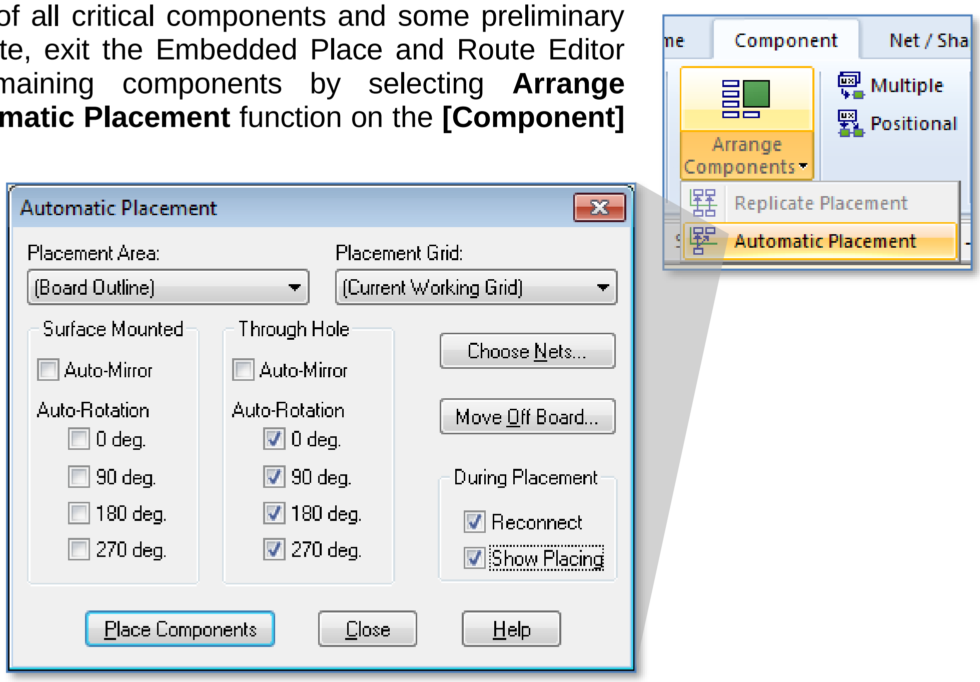
To set the default action, select the **Push→Options** dialog located on the **[Home]** tab



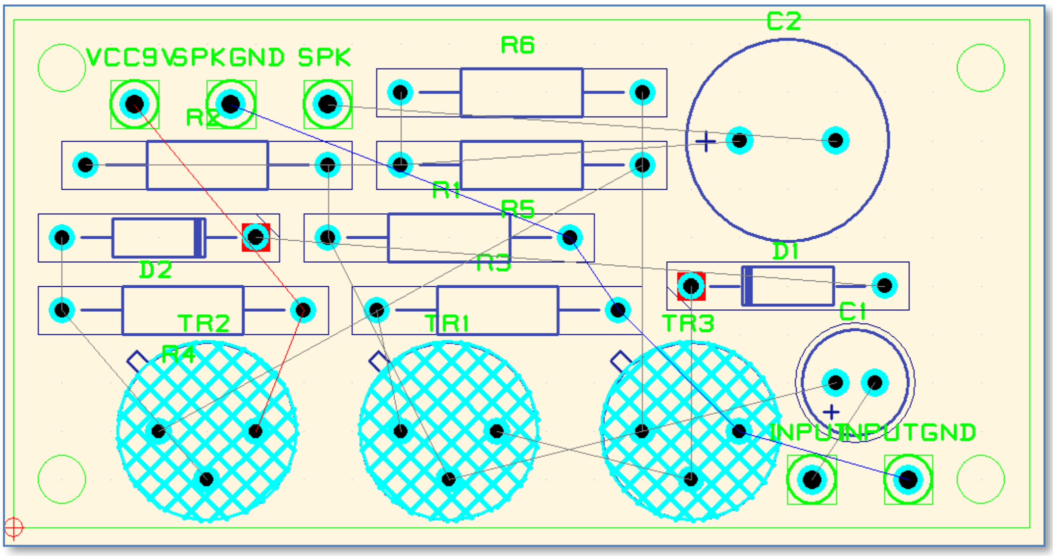
14. Place TR1, TR2 and TR3 like the image below. Practice using techniques to achieve some preliminary results.




15. After the placement of all critical components and some preliminary placement is complete, exit the Embedded Place and Route Editor and place the remaining components by selecting **Arrange Components→Automatic Placement** function on the **[Component]** tab.




*Enable* all *Auto Rotation angles* before placing the components (depending on your design rules). Try the different settings and experiment with the different results.




Sample placement with only o and 180 degree auto rotations enabled.

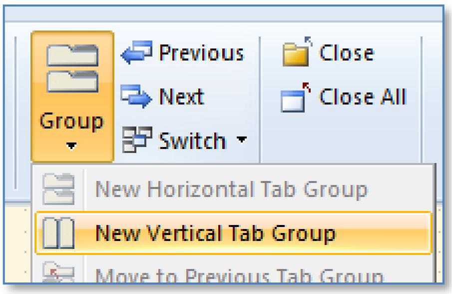
If you didn't manage to place the components, just open **DesignA3_CS.pcb** and save it as **DesignA3.pcb.**

16. Try moving the components manually using a finer working Grid 

(click on the grid button at the bottom of the window).

**Note:** you can select any footprint in PCB by simply selecting the particular symbol in the schematic. In CADSTAR, This called *Cross-Probing*. To try it, select **Group→New Vertical Tab Group** located on the **[View]** tab first. Then select any random item.

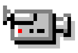
To continue with the next exercise, you should activate and enlarge the PCB Design window.



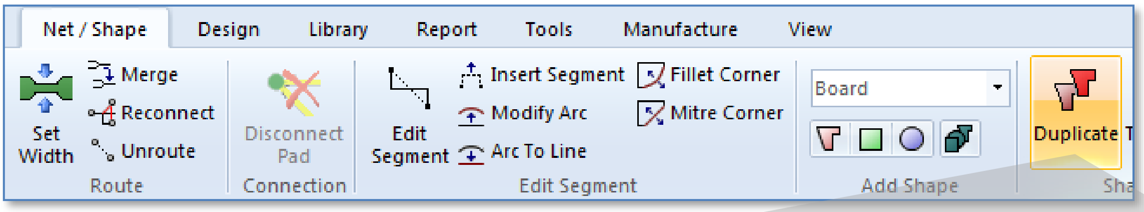
## Setting up Powerplane Templates for Copper Pour

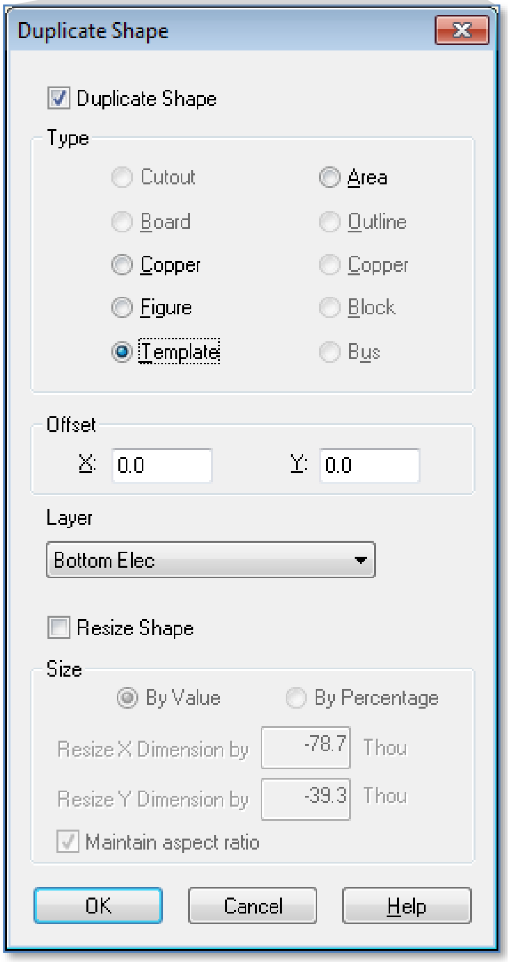
Power Planes are an integral element in the PCB. CADSTAR can accomplish this as a Negative Powerplane where templates can be created on designated Power Plane layers to set the boundary area for split power planes and DRC checking. This then requires a power plane output which is a traditional *negative* photo image output.

Alternatively templates can be created on Electrical layers for use as a positive photo image copper pour effect.  This guide will focus on this method as it is the most popular among users.



17. To create a partial power-plane, create a template by duplicating the board outline. Select board outline and then **Duplicate** shape function on the [**Net/Shape**] tab.




Change the type to ***Template*** and the layer to ***Bottom Elec***.

Disable **Resize Shape** if selected.

Click [**OK**] to create the template.

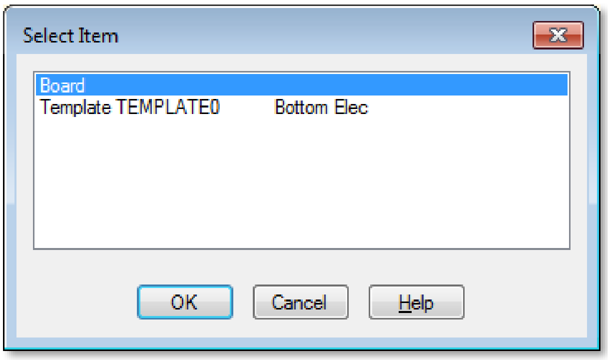
***Note:*** Copper pour will be generated automatically in the Embedded Place and Route or stand-alone Place & Route Editor on solder side based on the template area. Copper shapes will be created to fill in the empty space within the template outline connected, for example, to AGND.

18. After the template has been created you can set the properties to control how copper is generated. Select the template and click on the non-modal **Item Property** panel and pin it open.

**Note:** the demonstration video suggests **Bottom AGND** as a template name with signal **AGND**. Please set the properties as described below.

**Tip:** If you are unable to select the template, enable the pick from list function in the **[File]→Options [Interaction]** tab.

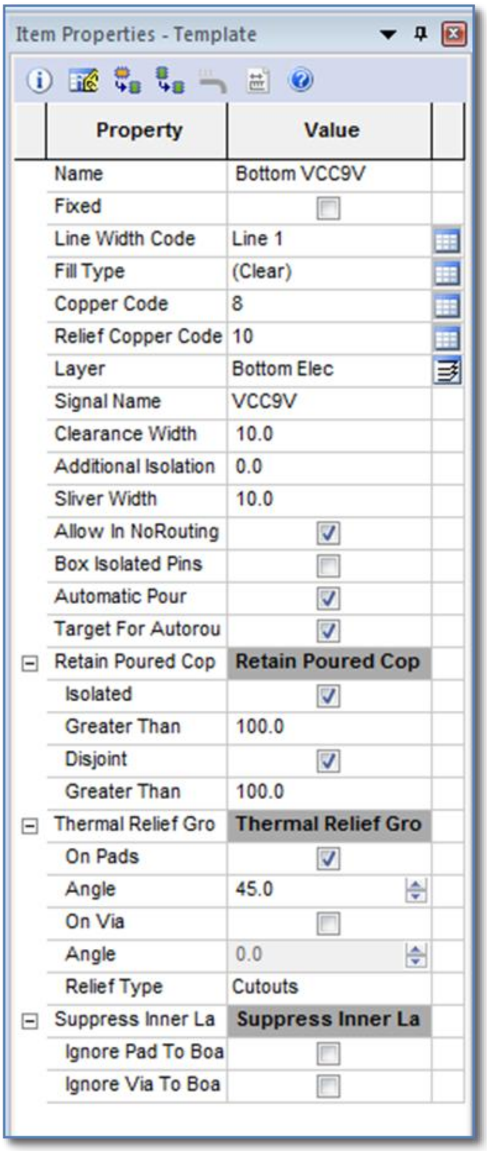
With this enabled, select the board shape outline once again. This time a *Select Item* dialog will appear to make it easier to select the template outline.




Set the properties as follows:

Name Template: Bottom VCC9V
Relief Copper Code: 10
Layer: Bottom Elec
Signal Name: VCC9V
Clearance Width: 10
Allow in No Routing [select]
Thermal Relief: Enable **On Pads**
Angle 45°

**Note:** *Automatic Pour is ENABLED!*
[These are the important parameters you need to set.]




19. Return to step 18 and repeat the process for the ***Top Elec*** layer using AGND for the template.

Set the properties as follows:
Name Template: Top AGND
Relief Copper Code: 10
Layer: Top Elec
Signal Name: AGND
Clearance Width: 10
Allow in No Routing [select]
Thermal Relief: Enable **On Pads**
Angle 45°

The steps that were mentioned in this chapter are again a typical sequence. There are other tools such as Radial Placement, Gate and Pin Swap, Replicate Placement etc., to help designers achieve correct placement of components.

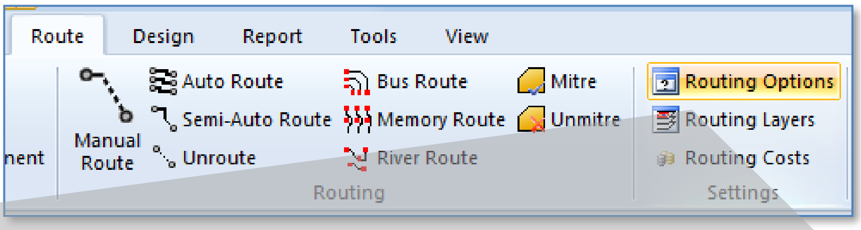
## Step 3 - PCB Routing for Design A

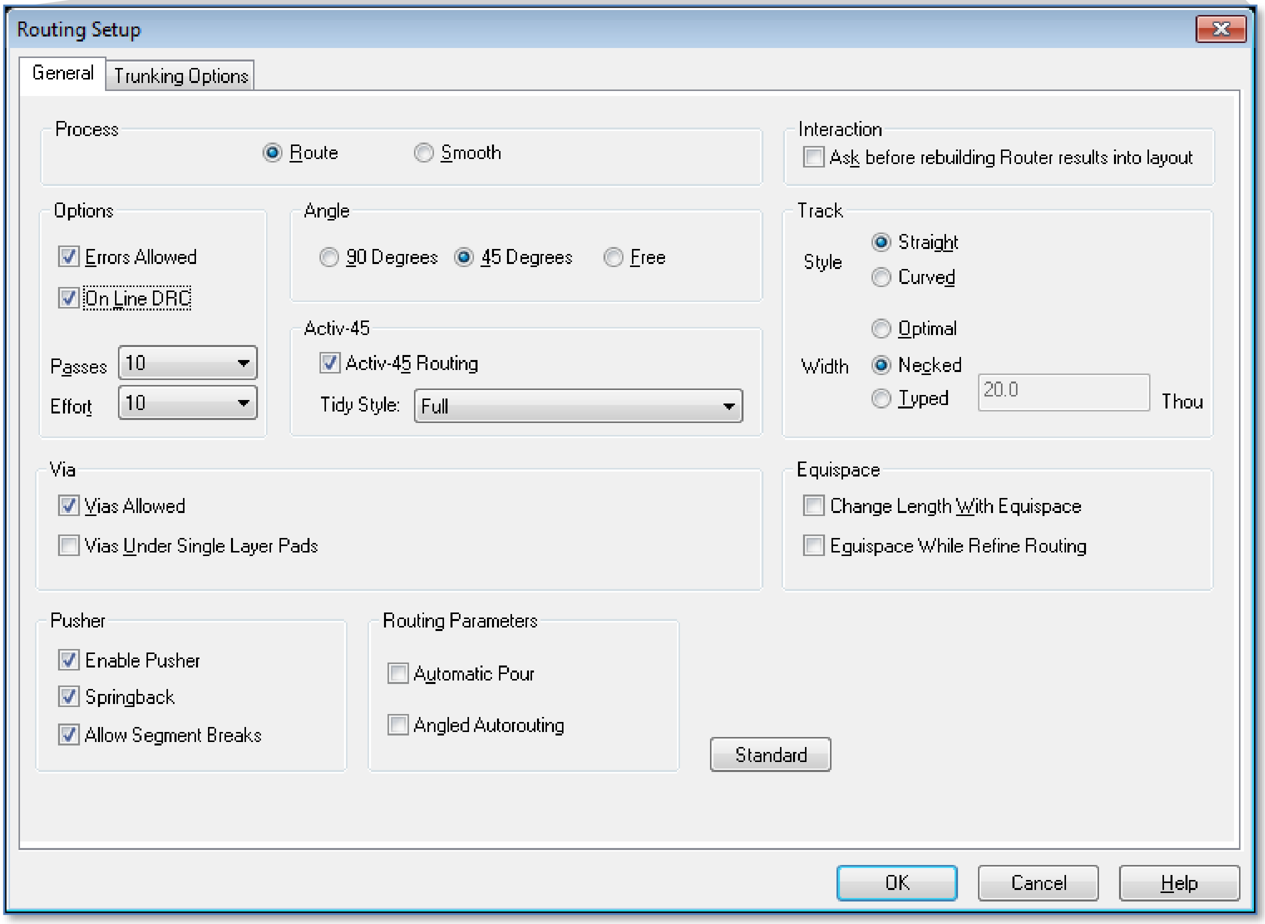
With placement completed we can now start to route the PCB. If you didn't manage to create the template, just open ***DesignA4_CS.pcb*** and save it to overwrite your current design before going to the routing environment.

1. Select the [**Tools**] tab→ **Embedded Place and Route**, to go to routing environment.

   Begin by check the **Routing Options**. Setting the Routing Options is very important before any routing.

   Select **Routing Options** button located on the **[Route]** tab

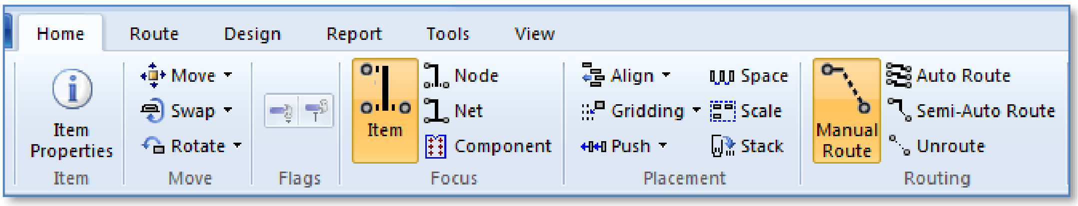



The **Routing Options** dialog contains several options to control routing behaviours:

Route Width, Routing Parameters (for autoroute), Routing Angle, On-Line Design Rule Check, Push Aside, Activ-45 Degree Routing etc.

Make sure that at least On-line DRC, Angled Autorouting, Angle 45 Degrees, Activ-45 Degree Routing are *Enabled*. You can use these options to create the result you want.



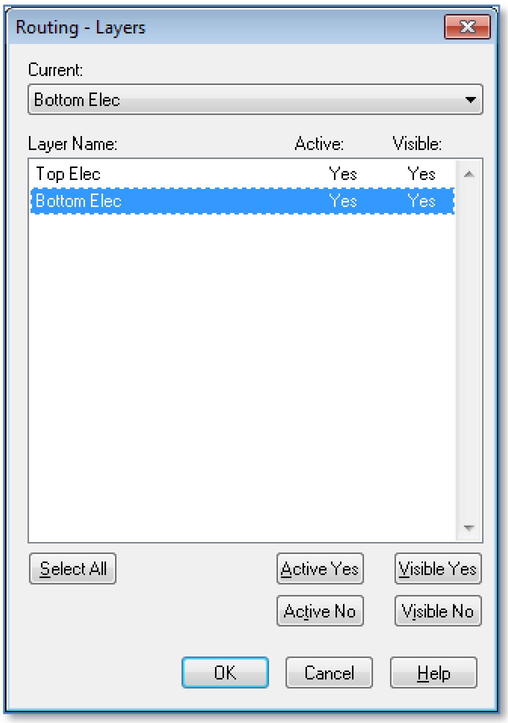

2. Start with manual routing by clicking two icons on the toolbar, **Item Focus** and **Manual Route** located on the **[Home]** tab as shown above.

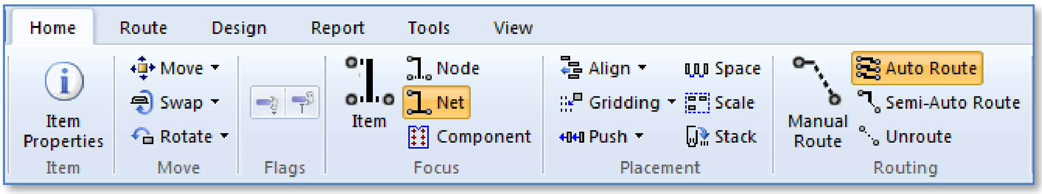
Try out the Activ-45 Degree Routing and Automatic Pour starting on the Solder-side (Bottom Elec), by selecting a net just once and moving the cursor to the other end of the net.

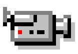
To insert vias, requires the changing of the active routing layer from *Top Elec* Top Elec to *Bottom Elec* Bottom Elec (by clicking the Top Elec button at the bottom of the window and changing the current layer to Bottom Elec).

While routing, you can insert a via by using the right-hand mouse button and select Change Layer.

Route width can be changed *on the fly* from Optimal to Necked or Change Width using the right-hand mouse button and select Change Width (you can choose a width between Min and Max, depending on your Route Assignments).



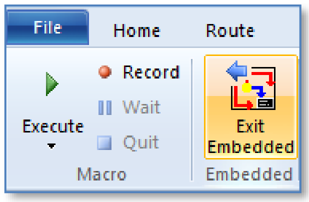
3. Use the automatic routing features. The two icons used are **Net Focus** and **AutoRoute** shown above**.** Nets can be automatic routed individually or by dragging a selection frame area around the whole board outline.

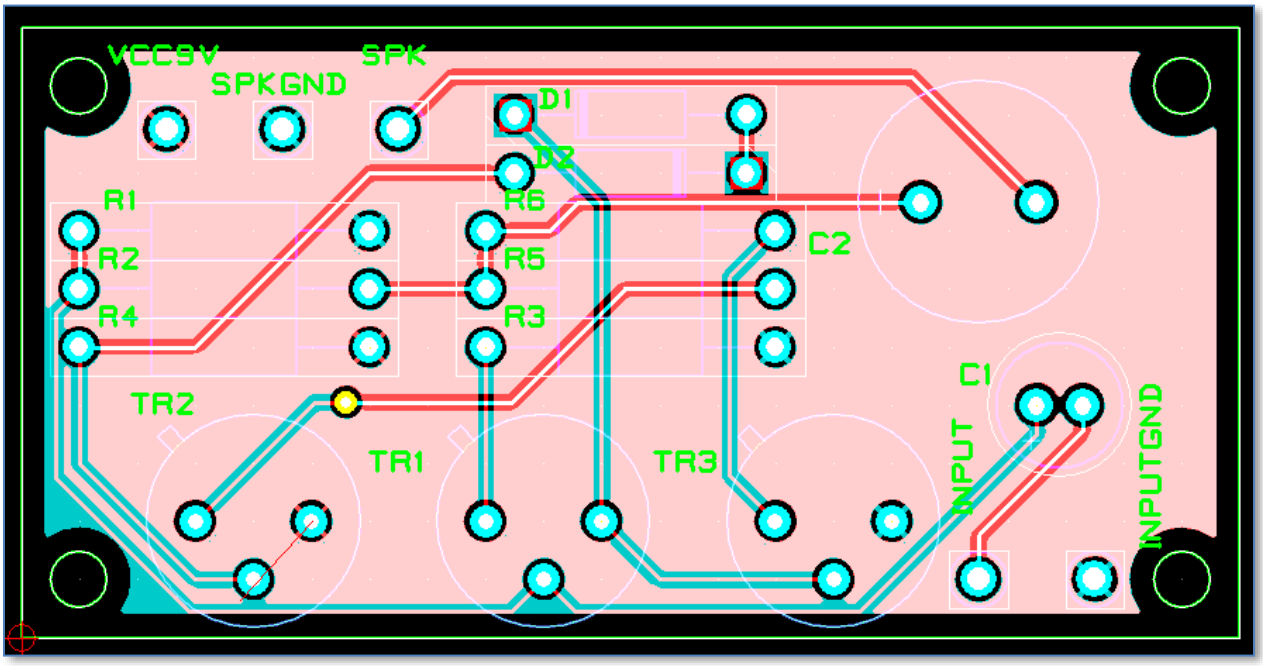
Copper pour will be generated automatically on the Top Elec and Bottom Elec layers since you enabled *automatic pour* earlier.

**Note:** the copper poured into the template will have followed the properties you have set. The copper will also have automatically avoided the cut-out of the board outline.

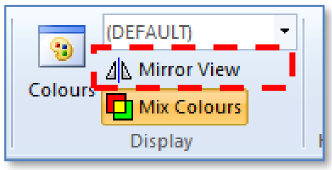
**Note:** Transistors, TR1-TR3 contain a round *Keep-out* area within the component shape, shown as cross-hatched in the previous images. You may choose to change the colour settings so that *component areas* are not visible. The settings for the templates that *Allow in No Routing* areas while be considered resulting in copper being poured within the area. Try it!

4. After completion, you can go back to the PCB Design Editor window by selecting **[File]** tab and clicking the **Exit *Embedded Place and Route*** icon. Don't forget to rebuild the router results into the layout. You can now see a design similar to the PCB shown below.




5. For a different view of the PCB use the Mix Colours (transparency) mode located on the [**View**] tab This will display multiple layers so that all items are visible. Shown above



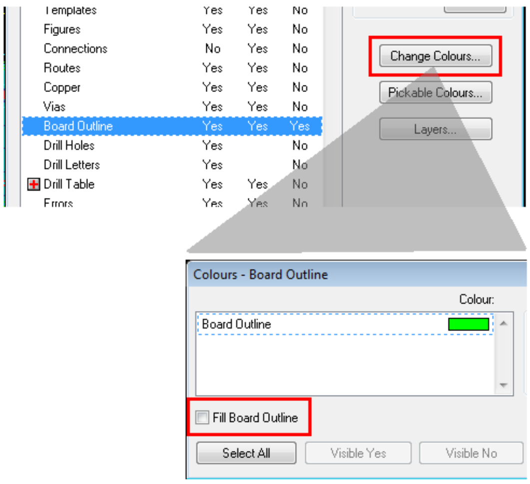

**Note:** This is best viewed using a black background.

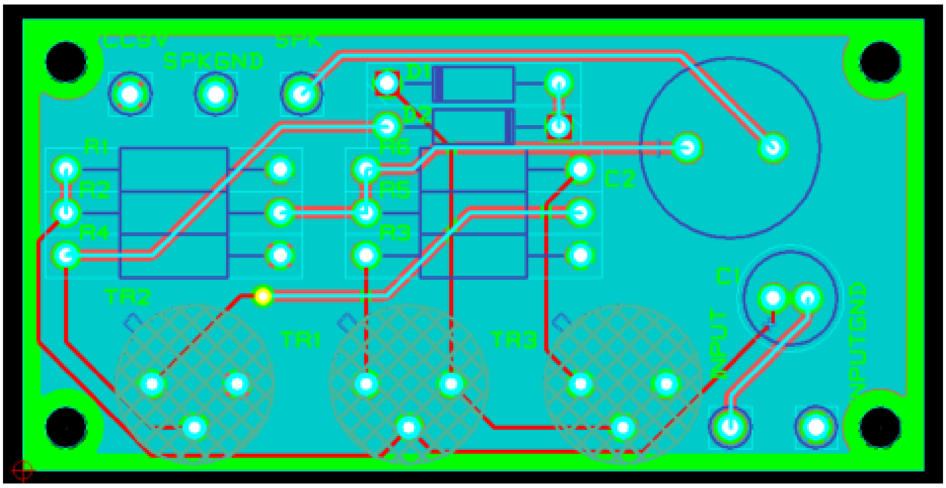
6. If you required, a mirrored view of the PCB design select [**View**] tab→**Mirror View**. This view option allows work to be performed as if you are working on the bottom side of the PCB.

7. The board can also be displayed filled. Select [**view**] tab -> **Colours,**

Pick the Board Outline category and select **Change Colours**

A checkbox in the Colours – Board Outline dialog allows you to toggle the fill style of the board.





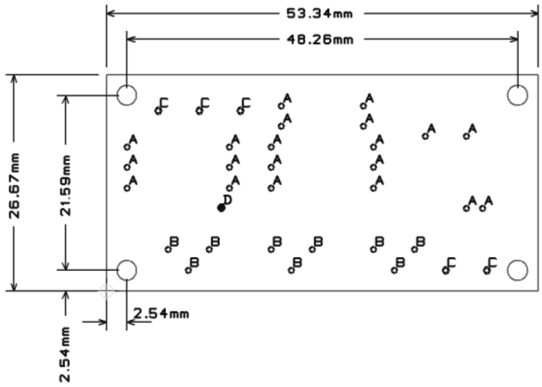

8. Save the file

If you didn't manage to route the design, just open **DesignA5_CS.pcb** to have a look.

This is probably the last stage of the PCB design. It requires some careful considerations as to how the board can be routed, what are the critical nets and what nets have to be routed manually etc. For advanced users, more routing features and high-speed routing are to be considered.

## Step 4 - Manufacturing data for Design A

At this stage, you can also create the manufacturing data (Gerber, N.C.Drill, Parts List, Placement data, Drill Drawing, etc.) for the manufacturing of the PCB. Start by creating a Drill drawing with an associated Drill table as shown below. Your design may be different.



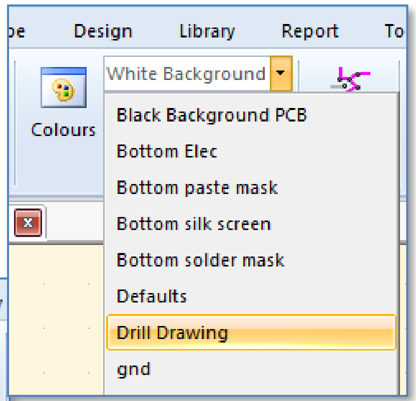

| Drill Table | | | | |
|---|---|---|---|---|
| Size | Plate Through | Letter | Count | Tolerance |
| 0.50 | YES | D | 1 | +/- 0.02 |
| 0.70 | YES | B | 9 | +/- 0.02 |
| 0.80 | YES | A | 20 | +/- 0.02 |
| 1.00 | YES | C | 5 | +/- 0.02 |

Drill holes marked with letters that correspond to a hole count in a table or legend.

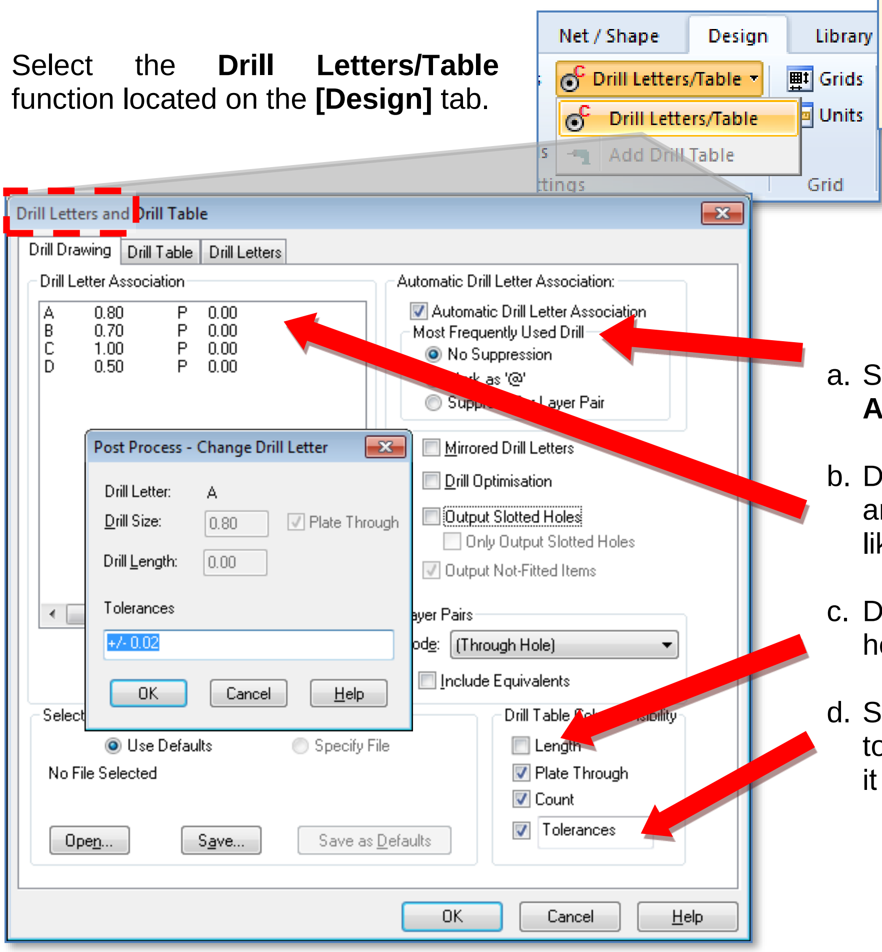
1. Change the preferred units to mm with 2 decimal places.

2. Load the colour file called **Drill Drawing**. This is found in the pull-down menu adjacent to the colour palette Icon found in the [**View**] tab.

   This can also be loaded by typing **[col drill drawing <enter>]** at the command line.




3. Select the **Drill Letters/Table** function located on the **[Design]** tab.




a. Select **Automatic Drill Letter Association** option as shown.

b. Double click on the Drill Letters and enter a tolerance comment like ***+/- 0.02***.

c. Deselect the **Length** column header

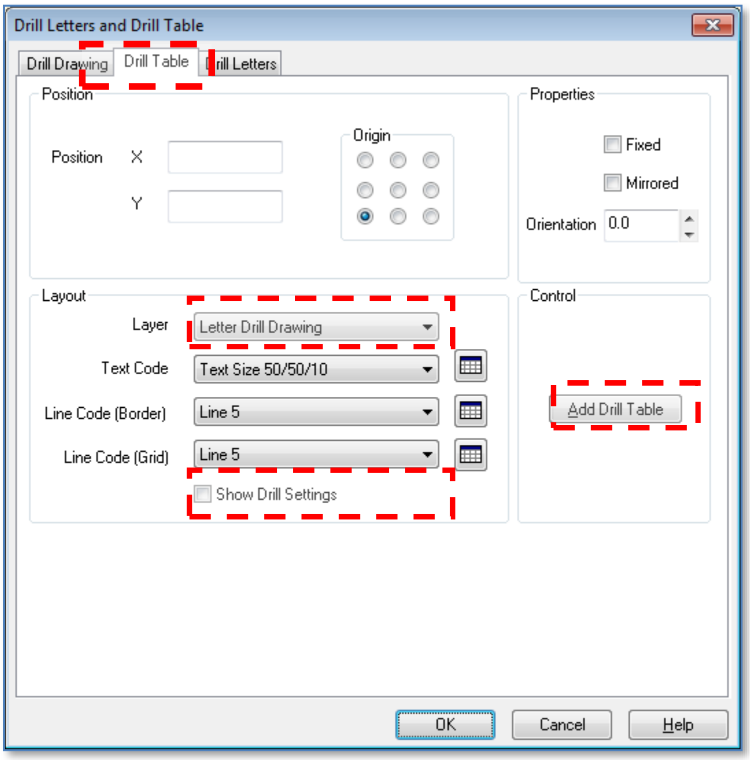
d. Select the **Comments** column to appear on table and change it to “**Tolerances**”

4. Select the **[Drill Table]** tab.

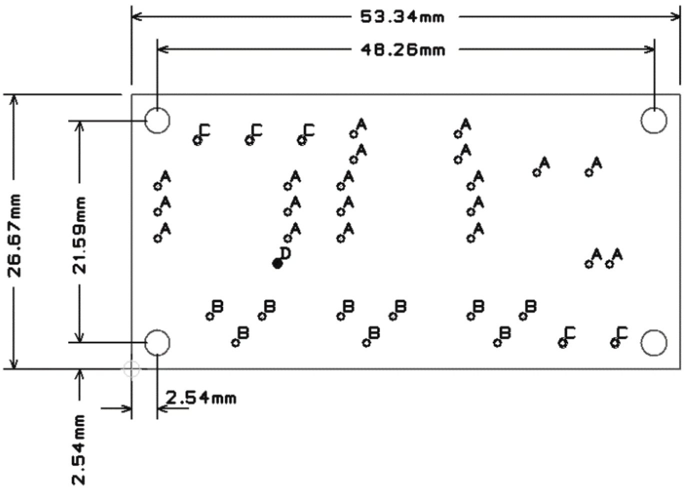
   a. Change the Layout, layer to Letter Drill Drawing

      Selecting the *Show Drill Settings* option will show pertinent settings that are useful for the Fabrication of the PCB. Leave it deselected.

   b. Click to [Add Drill Table] button. This will make the drill table appear on your cursor.

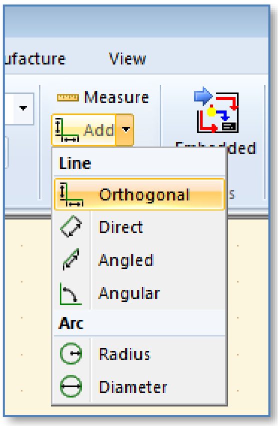



5. Move the table to the right of the PCB board outline and <click> to release it as shown below.

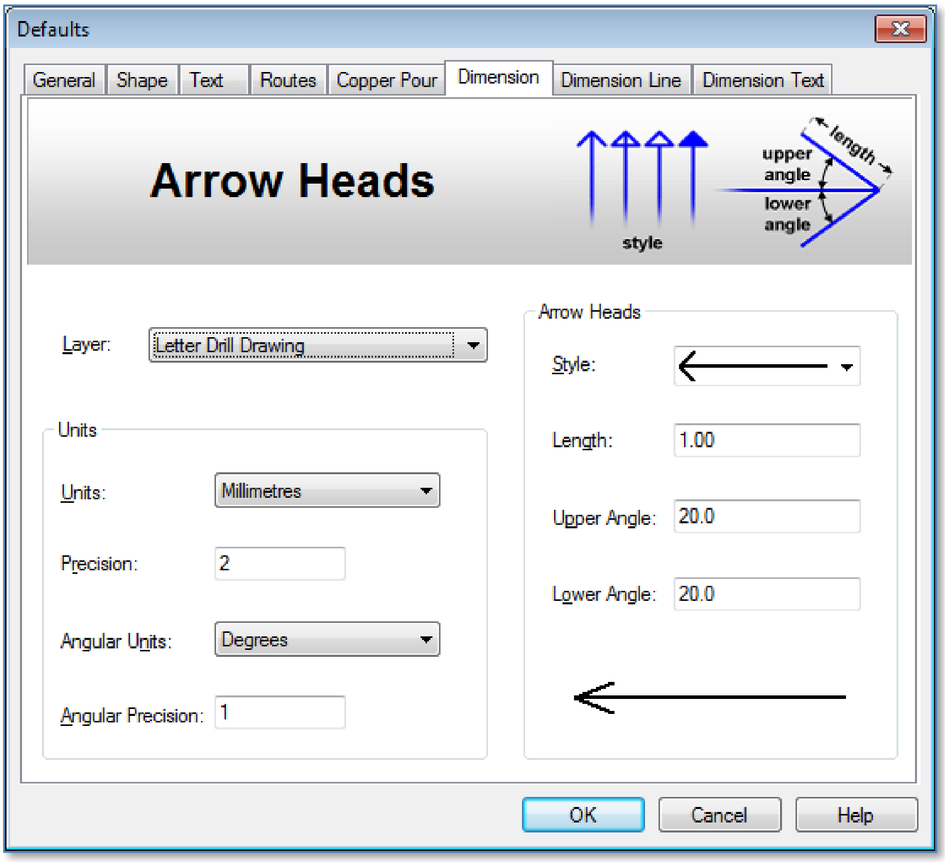


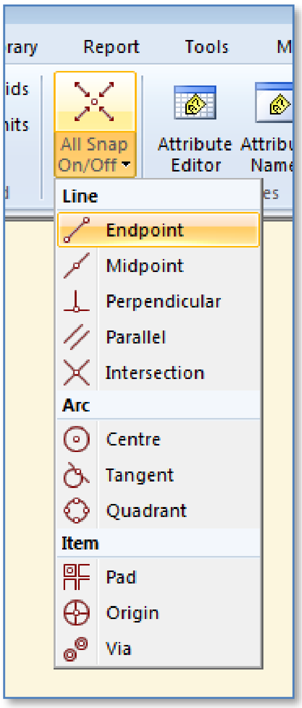

| Drill Table | | | | |
|---|---|---|---|---|
| Size | Plate Through | Letter | Count | Tolerance |
| 0.50 | YES | D | 1 | +/- 0.02 |
| 0.70 | YES | B | 9 | +/- 0.02 |
| 0.80 | YES | A | 20 | +/- 0.02 |
| 1.00 | YES | C | 5 | +/- 0.02 |

6. Try adding dimensions as shown on the previous page by clicking the [**Home**] tab and then selecting the style of dimension you wish to add from in the **Add Dimension** list.



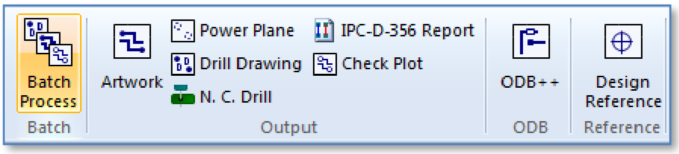

The default dimension styles and details are declared in [**Design**] tab, **Defaults** dialog. Once the dialog is displayed, move the cursor over the various parameters for a graphical representation of the meaning.



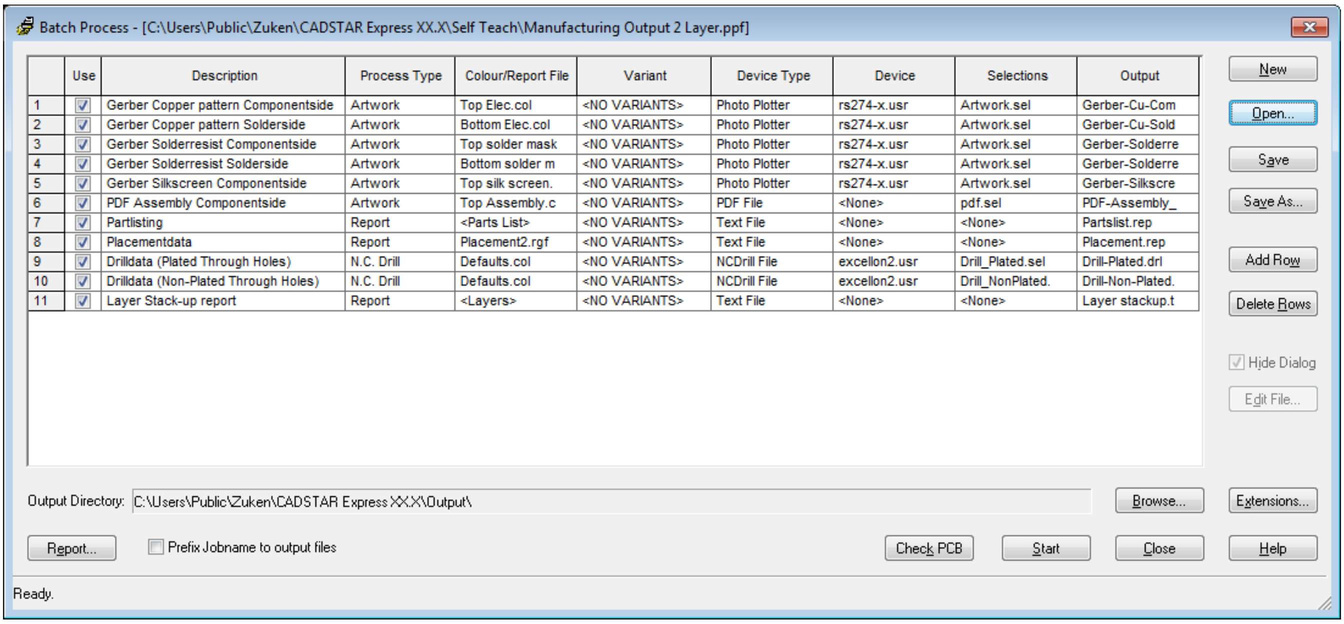




TIP: Try using the *Snap* mode functions located on the [**Design**] tab when adding dimensions. →

7. Select the **[Manufacture]** tab and click the **Batch Process** button on the ribbon.




8. In the Batch Process window, select [Open] and choose Manufacturing Output 2 Layer.ppf, which you can find in the ../Self Teach/ directory.



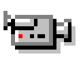

In this 2 Layer design, the layers that are to be generated are;

- *Top Elec*
- *Bottom Elec,*
- *Top Solder Mask,*
- *Bottom Solder Mask*
- *Top Silkscreen*

(all in Extended Gerber RS274-X format).

Additional data generated by CADSTAR manufacturing are;

- *Parts Lists,*
- *Layer Stack-up report*
- *Placement Data*
- *Drill Drawings (in the case of this design is recommended to produce PDF artwork of the Drill Drawing layers) rather than let CADSTAR generate a non-WYSIWYG output file.*
- *Extended Drill Data.*



← Click the demonstration video link to see how additional rows can be added such as for a drill drawing PDF file.

9. Click [START]. All manufacturing data will be saved in the Output directory.

**Note:** During the generation of the manufacturing data, a check is performed to ensure items such as Areas, Templates and Component Area are not visible. If they are visible in your design you may receive warnings on rows that are using a colour file. To fix this, exit the ***Batch Process*** dialog and then load the colour file for the row that is being flagged as a warning. Check the colour file and change the visibility settings to **Off** for the item category being flagged. Return to the ***Batch Process*** function and click the button to [**Check PCB**]. This is to check the colour files for items that are not normally output as manufacturing details.

**TIP:** Select the Prefix Jobname to Output Files control to append the name of the design to each output file. This makes it easier to keep manufacturing output for different designs in the same folder.

There are other tools such as *Associated Dimensioning (Orthogonal, Angular, Radial etc.), Snap, Component Rename* etc., to help designers like you to create all the necessary manufacturing data.

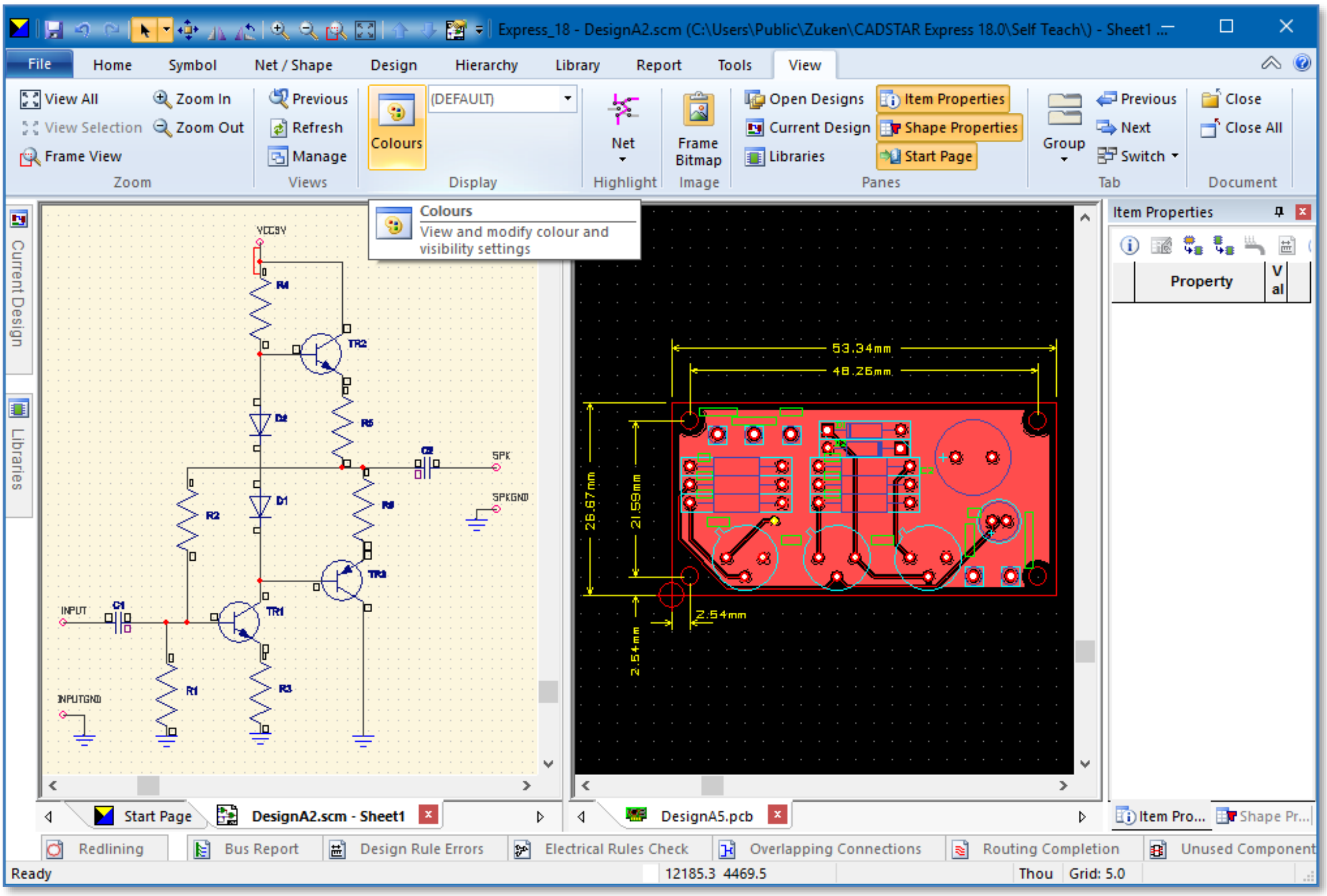
**TIP:** CADSTAR also provides Design Rule Check functionality. When you run this function, DRC errors will be flagged in the PCB layout. If you have unresolved errors at the time of post processing, the Manufacturing output will notify you.

CADSTAR

## Step 5 – Saving your Design for future Reuse

Small schematic and PCB designs like this Amplifier are typical examples of circuits that are saved for future reuse. Once saved as a reusable circuit they can be recalled for use with other designs. CADSTAR offers functionality for managing *reusable circuits*.

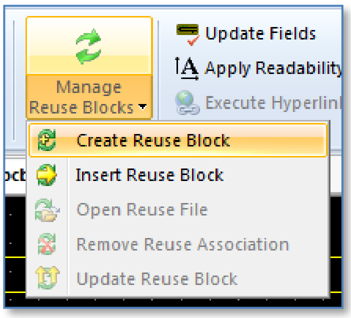
1. Display both your Schematic and PCB Design in CADSTAR.

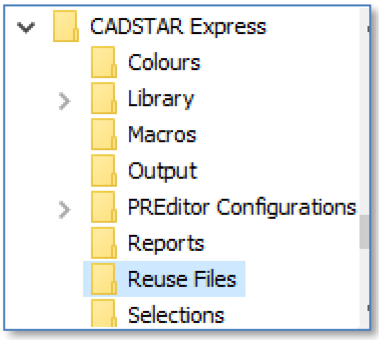



2. Open the ***Colour*** settings for the design and change the settings for board outline, figures and dimensions to ***non-pickable***.

3. Select all the electrical contents of your PCB using a simple framing method. If Cross-Probing is active the same components and nets should be selected in the schematic window. Deselect the SOLDEREYE parts.

4. Select from the **[Design]** tab **Manage Reuse Blocks→Create Reuse Block**. The default location for reusable blocks is in the Reuse Files folder as per the Path locations defined in the **[File]** tab **→Options** dialog.





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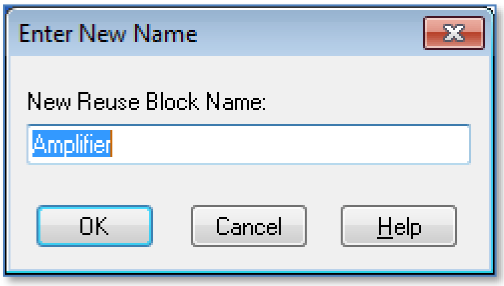
5. Choose a valid meaningful name for the file. I.e. "**Amplifier"** and then click **[OK**].

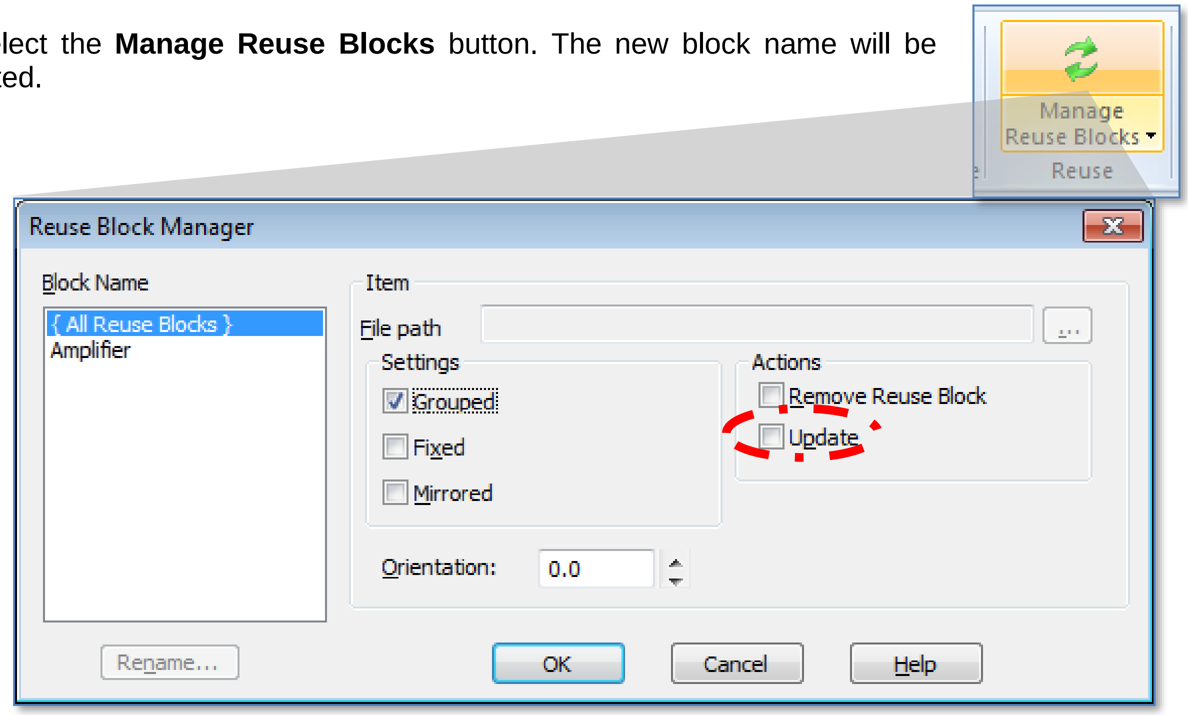
6. Enter the same name for the Reuse Block name and then click **[OK**]




7. With the schematic data still selected from cross probing, carefully click the schematic window tab. (not within the window since this will deselect the contents). This will change the tool ribbon used for schematics. Reselect the circuit block and select **[Design]** tab **Create Reuse Block**.

   If you have prematurely clicked and deselected the circuit repeat the process for the schematic data. Give the schematic reuse block the same name as the PCB reuse block i.e. **Amplifier.scm. Do not include the SOLDEREYE parts.**

8. Select the **Manage Reuse Blocks** button. The new block name will be listed.




**Note:** Since the Reuse Block files are named, this functionality will allow you to manage them within the \Reuse Files\ folder. If you decided to make changes to the blocks, update both the Amplifier SCM and PCB files. Then, for any design that used the Amplifier circuit, you can simply update them by double clicking on them and selecting the **Actions – Update** option shown above.

In the next project, Design B, the Amplifier reuse blocks will be used. Simply select from the [**Design**] tab, **Manage Reuse Blocks →Insert Reuse Block** and select **Amplifier.**

CADSTAR

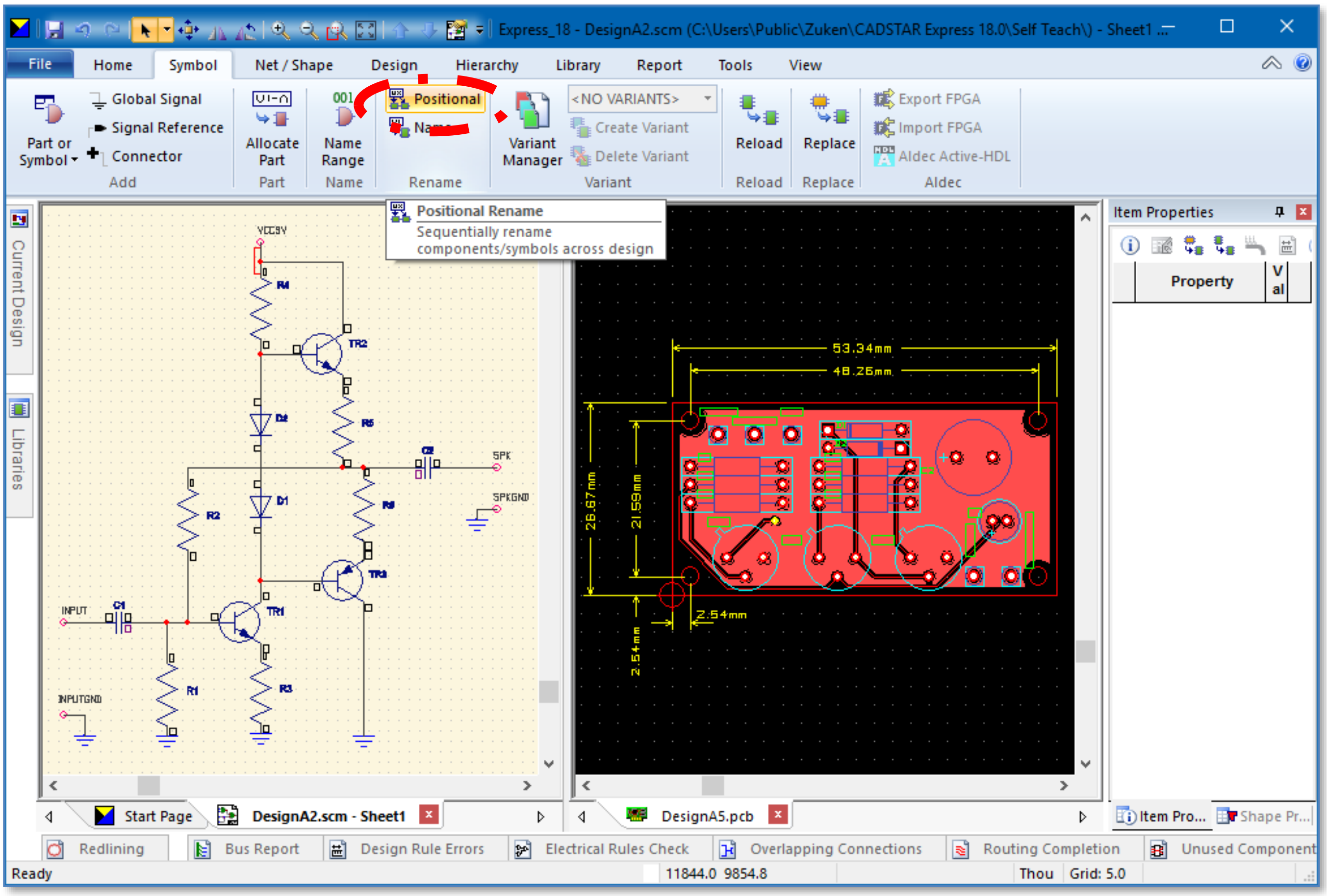
## Assigning Unique Reference Designators for Reuse Circuits

Before reusing these circuits we recommend you perform a reference designator *renaming* procedure. This will assign unique reference designators to the schematic and PCB components used in the reuse circuits blocks and will also help to eliminate the chances they will be renamed automatically by CADSTAR when they are inserted as reuse circuit blocks.

For instance; When inserting a reuse block into a schematic or PCB that may already have used the reference designators that are used in the reuse definitions, CADSTAR will resolve the duplicate reference designators automatically by renaming them to the next available ref des. This can cause the reuse circuit blocks to become out of synch in between the schematic and PCB reuse blocks.

An elegant solution is to use the rename component function to rename the used reference designators to something with a higher level prefix. I.e. R1 → R1001, C1 →C1001.

9. Open the **Amplifier** Schematic and PCB so you can see both at the same time and then click in the schematic window to make it active.




10. Select the Positional Rename button on the **[Symbol]** tab as shown above.





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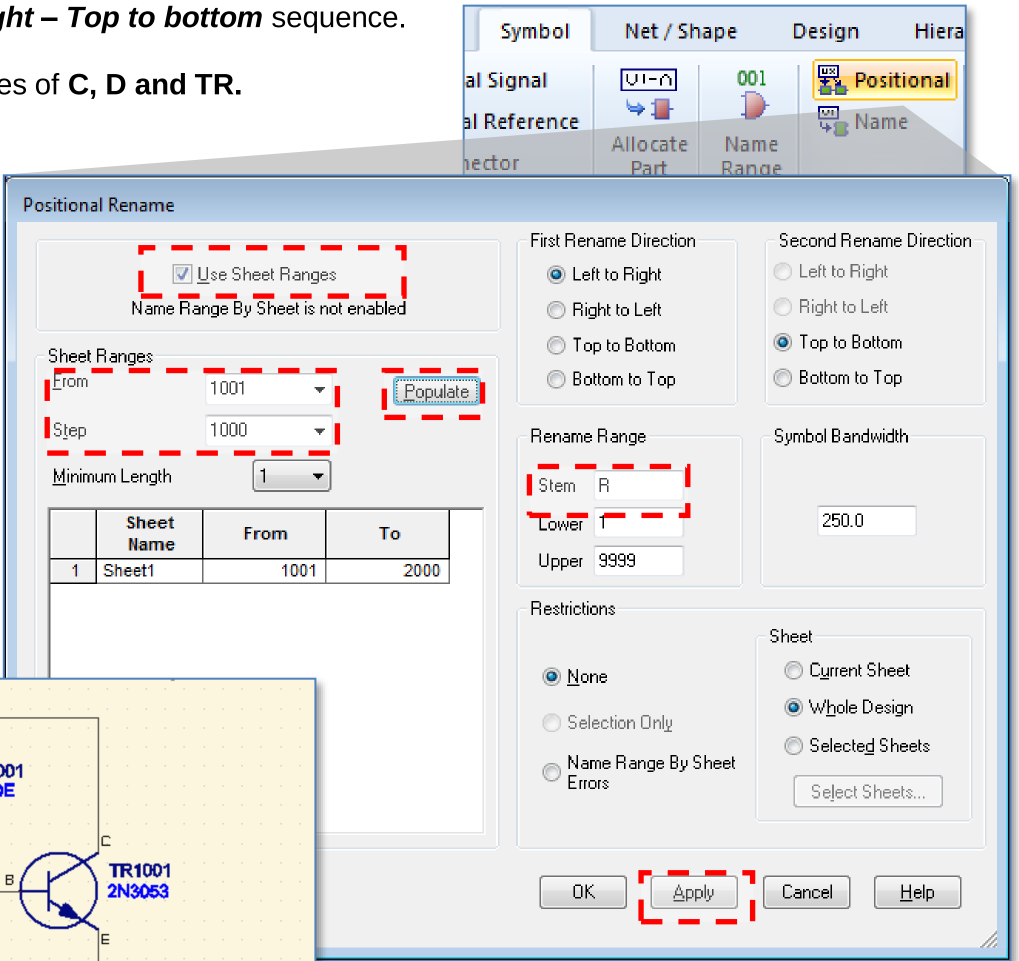
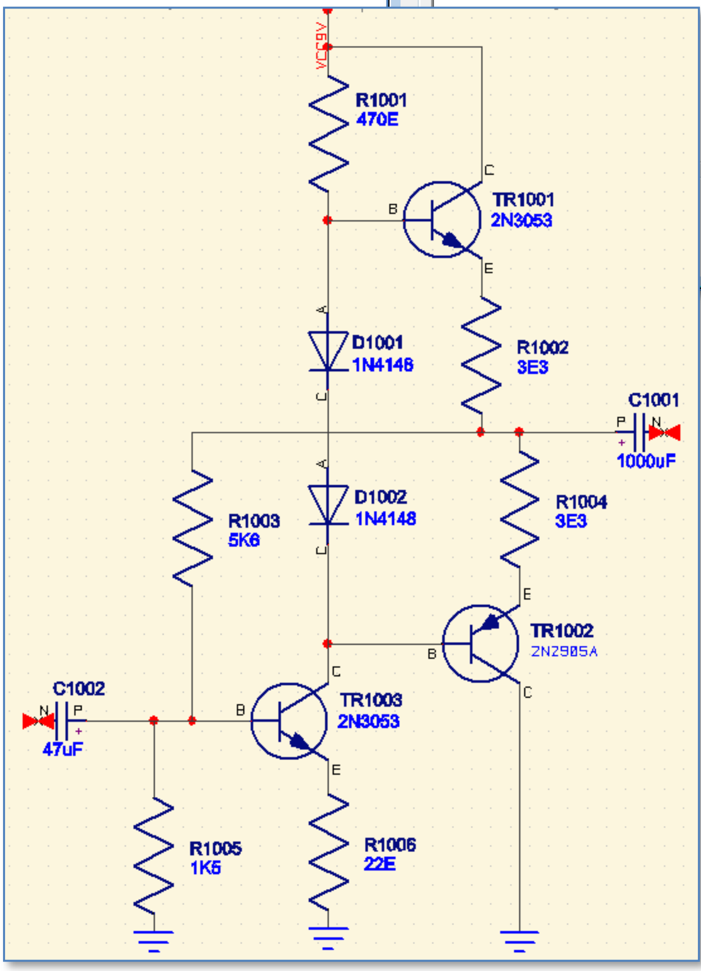
11. Apply the settings as shown in the image for components with a stem name of **R.**

This will rename the resistors using a 1000 prefix range in a ***Left to Right – Top to bottom*** sequence.

Repeat for stem names of **C, D and TR.**



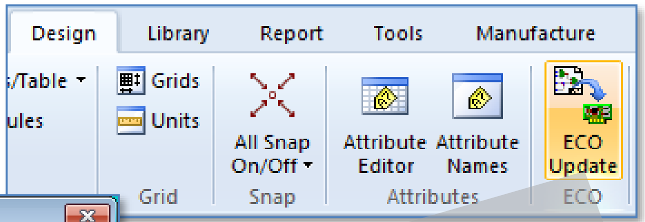

12. Save the Amplifier schematic again, overwriting the version currently in the ***Reuse Files*** folder.

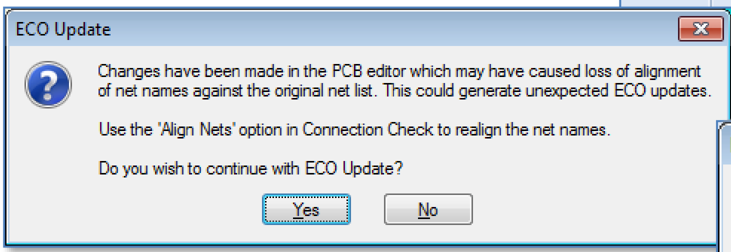
The renaming of the components in the schematic can now be passed to the PCB circuit block by way of the **ECO Update** function.

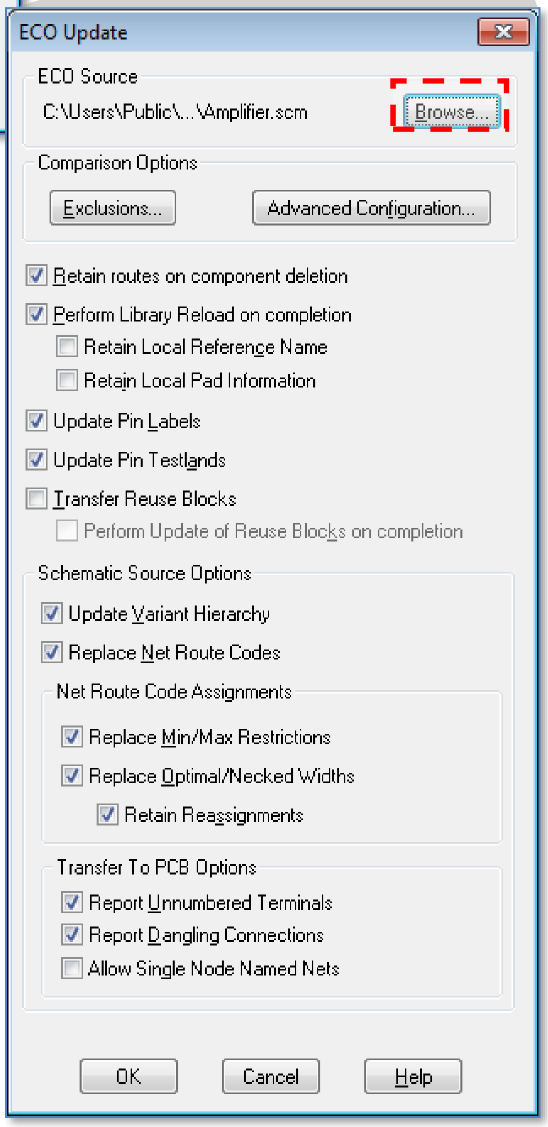
13. Click in the PCB window for the Amplifier to make it active.

14. Click on the [**Design**] tab and then the **ECO Update** button.

    Click **[Yes]** if the following dialog appears.



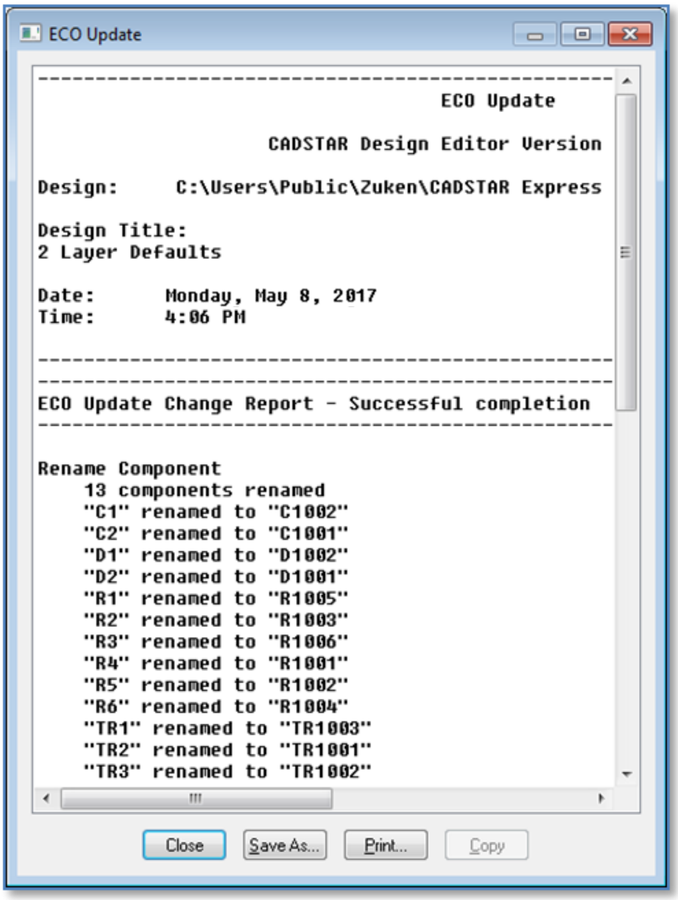




15. Browse to the \Reuse Files\ folder and select the **Amplifier.scm** as the *ECO Source data*.

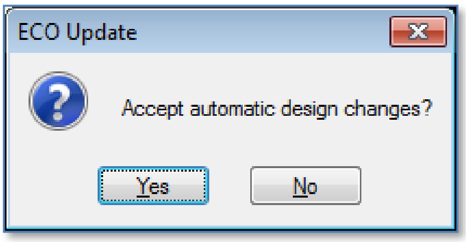
16. Apply all other settings as shown and click the [**OK**] button.

17. Click **[Yes]** on the *Design Comparison information* dialog. The results will be displayed in an ECO Update report



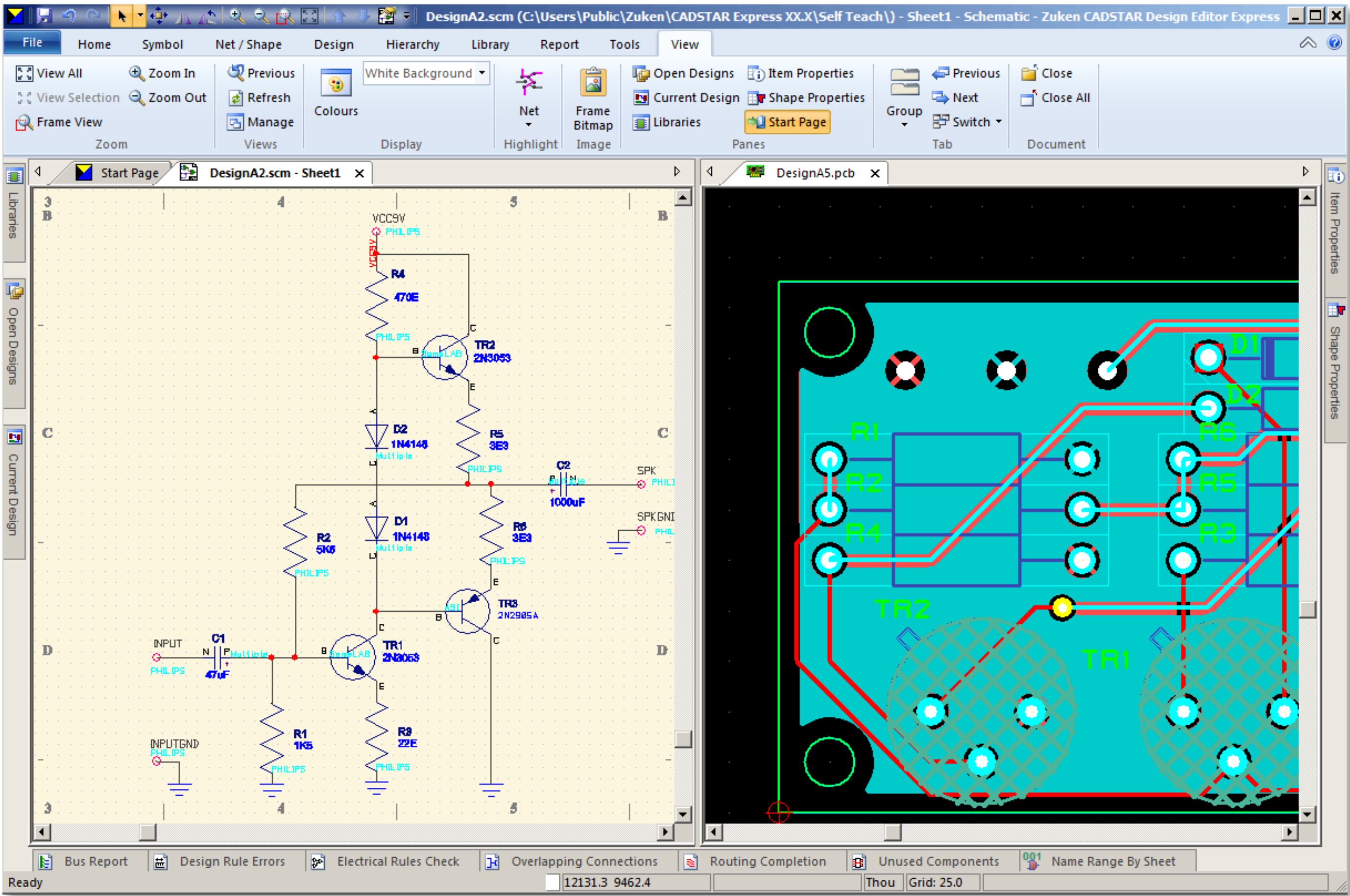

**Note:** ECO Update will also change system assigned net numbers as part of the process. If you have important nets it is recommended they be given proper names.

18. After reviewing the report carefully, click the **[Close]** button. You will be presented with opportunity to accept the changes. Click **[Yes]**




The PCB design will now be updated to match the schematic.

19. Save the Amplifier PCB design again, overwriting the version currently in the \Reuse Files\ folder.



**This completes the first design with CADSTAR Express!**

CADSTAR

## Add the Power of 3D to your Design

You can also check out BoardModeler Lite, supporting import/export of STEPS AP203, AP214, ACIS,STL and IDF formats, providing you an optimized solution for the placement and verification of a PCB Design in its own 3D environment, including:

a. Replacing board shapes and modifying component placements which are smoothly back annotated.

b. Creating detailed 3D models using the 3D parts creation wizard

c. Importing Mechanical Enclosures (or other PCB designs).

d. Measuring Distances and Checking Clearances.

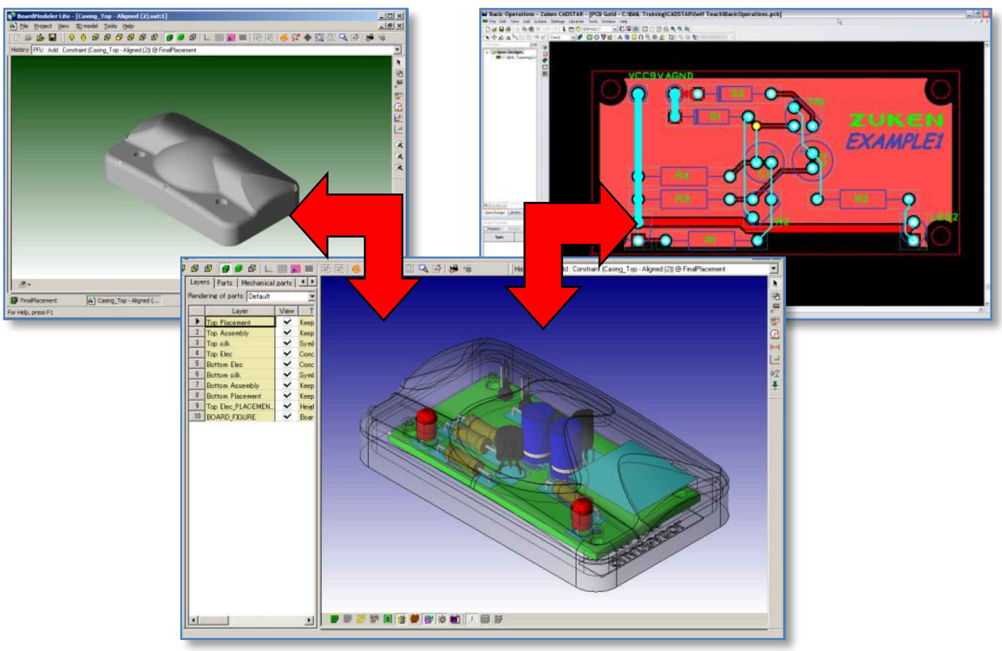
e. Running Batch collision checks.

BoardModeler Lite ***is more than just a 3D viewer!!!***

You can find more information at:

https://www.zuken.com/en/product/cadstar/bundles/

Mechanical CAD CADSTAR

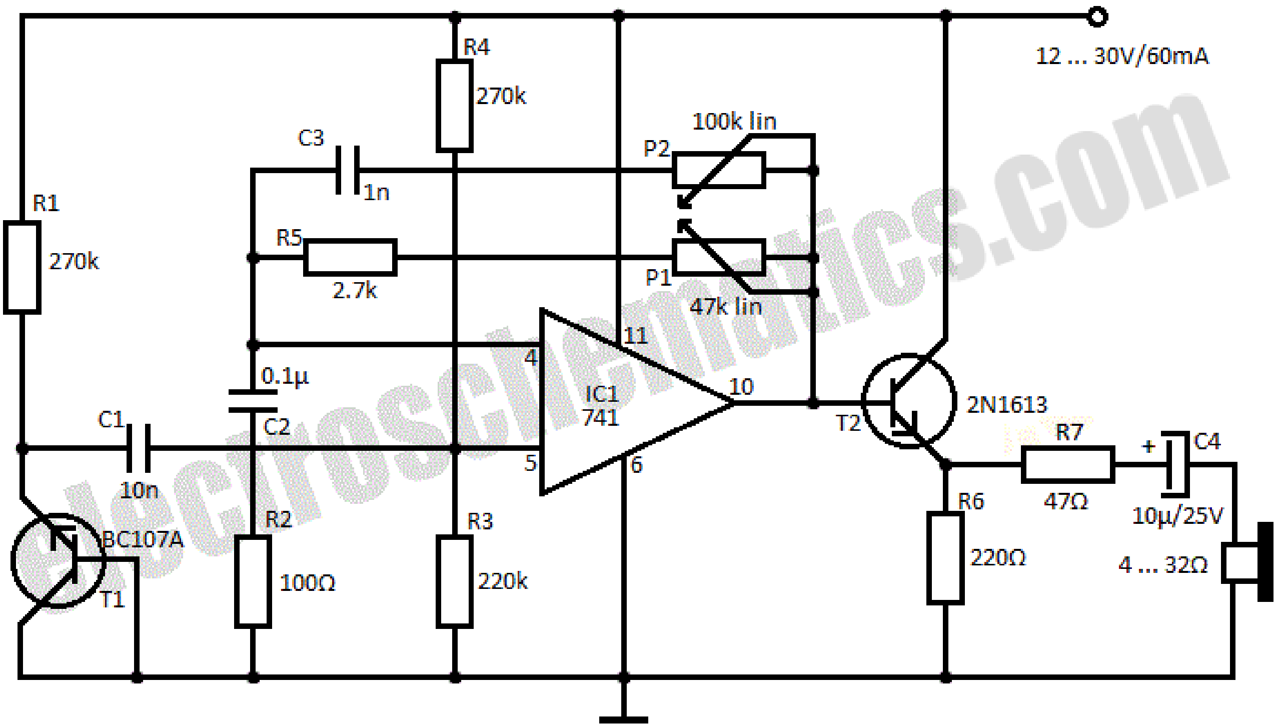


## Chapter 2 – Design B

In Design B, we will expand on what you have learned in **Design A** by exploring more features within CADSTAR. We will use the Amplifier circuit in the form of a Reuse Block for both the schematic and the PCB design. We will use Hierarchical features in the schematic and use a more elaborate PCB board outline with predefined component placement as an example of a Mechanical CAD driven system.

The project we will be designing is an audio device that many electronic hobbyists have built to cure insomnia. The circuits will emulate the sound of rain falling. This is similar to that of a white noise generator.

The original circuit was obtained from www.electroschematics.com as a free download.



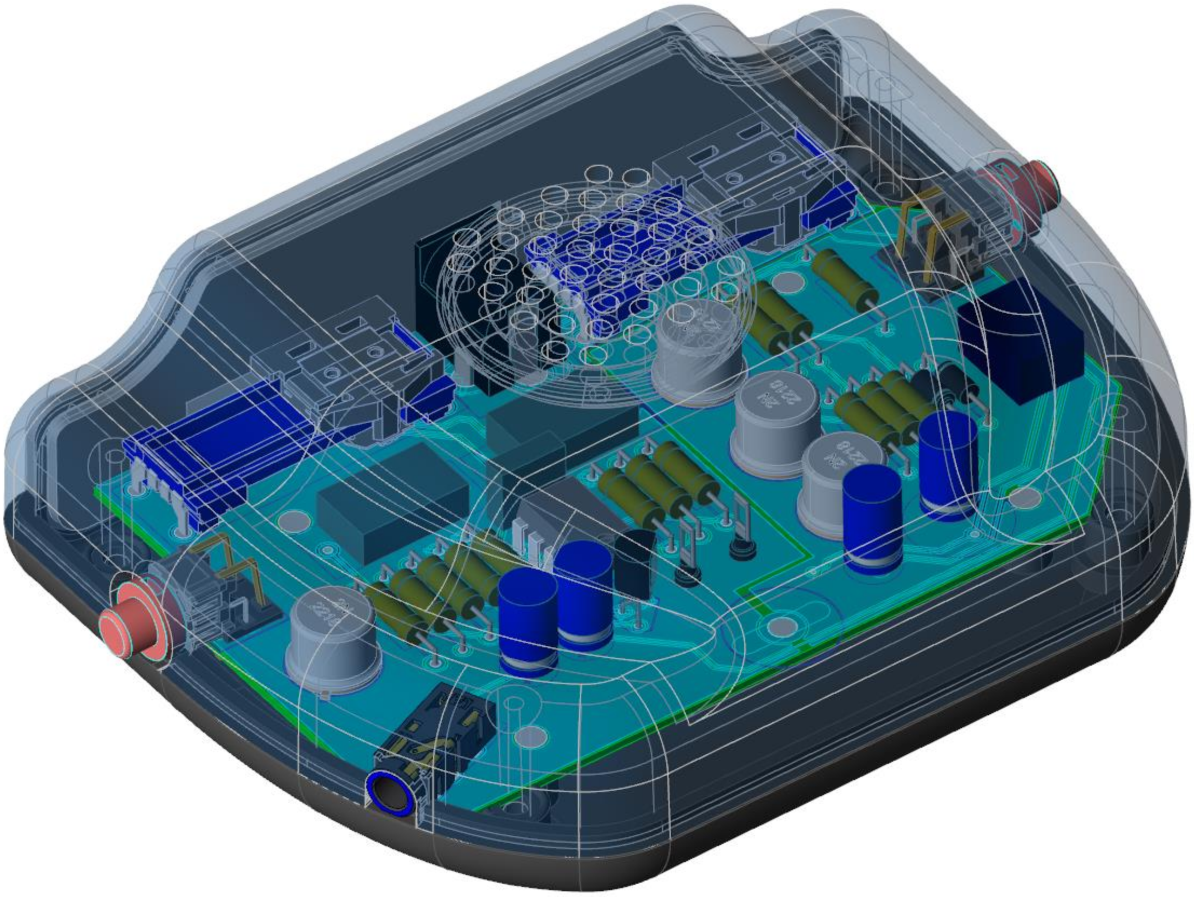

We have expanded on this by adding an additional amplifier that will be activated with the push of a button and an optional ear phone jack.

The PCB design will be created for you with predetermined coordinates and rotations of the parts. You will import this as a DXF file and begin placing the remaining parts.

Routing and Placement can be accomplished using the Embedded Place and Route Editor.

You will then be able to use your new skills from the previous design to complete Design B called *Rainmaker*.

The Image below contains the finished Rainmaker PCB design. The 3D models are available as part of the CADSTAR – Board Modeler Lite tutorial guide.  If you would like to take this project to the 3D Level contact your CADSTAR Sales agent to obtain a full CADSTAR and Board Modeler Lite evaluation license.



## Step 1 - Schematic for Design B

The sequence steps are the same as Design A.

1. Create a new schematic sheet using **Form A3-euro**. Set the working grid to **thou** and screen grid to **100, 100.**

2. Pick out components from the Library Workspace window. You may also use the Library Searcher as well.

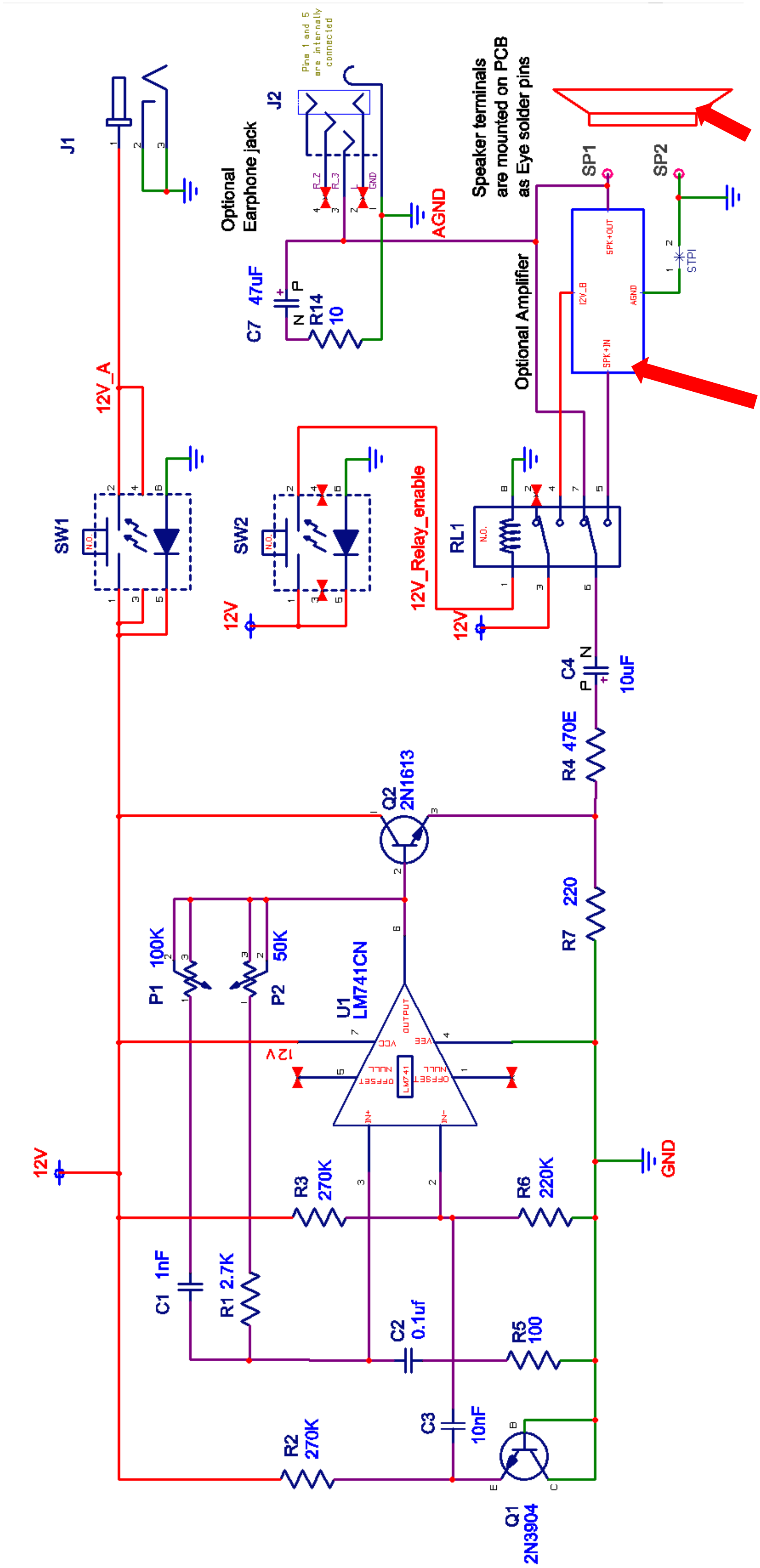
   The Parts list is as follows

| Part Name | Description | Qty | Comps. |
|---|---|---|---|
| 0.1UF-COG2-5% | 0.1uf 100V COG Mlayer Ceramic | 1 | C2 |
| 10-TR4-1% | 10 Ohm TR4 Metal Oxide Film 1% | 1 | R14 |
| 100-TR4-1% | 100 Ohm TR4 Metal Oxide Film 1% | 1 | R5 |
| 10UF-10V-EC | 10uF 10V Electrolytic Capacitor | 1 | C4 |
| 2.5MM PWR CON | Power supply connector 2.5mm | 1 | J1 |
| 220E-TR4-1% | 220 Ohm TR4 Metal Oxide Film 1% | 1 | R7 |
| 220K-TR4-1% | 220K Ohm TR4 Metal Oxide Film 1% | 1 | R6 |
| 270K-TR4-1% | 270K TR4 Metal Oxide Film 1% | 2 | R2-3 |
| 2K7-TR4-1% | 2.7K TR4 Metal Oxide Film 1% | 1 | R1 |
| 2N1613 | SABER TRANSISTOR | 1 | Q2 |
| 2N3904 | SABER TRANSISTOR | 1 | Q1 |
| 47uF-10-EC | 47uF 10V Electrolytic Capacitor | 1 | C7 |
| 470E-MRS25-1% | Metal film resistor MRS25 470E 1% | 1 | R4 |
| BA156K0103J-- | Leaded film capacitor | 1 | C3 |
| BA156K0104J | 1nf Leaded film capacitor | 1 | C1 |
| LM741CN | SINGLE OPERATIONAL AMPLIFIER | 1 | U1 |
| LGY2109-1701F | STEREO- CONNECTOR - EARPHONE | 1 | J2 |
| NEC_TOKIN_UC2_RELAY | NEC TOKIN's UC2 Mini Signature relay | 1 | RL1 |
| RS15H11AA04M-100K | Slim Slide(Slim 4) RS**H Series 100K | 1 | P1 |
| RS15H11AA04M-50K | Slim Slide(Slim 4) RS**H Series 50K | 1 | P2 |
| SOLDEREYE-1MM | Soldereye 1.0 mm | 2 | SP1-2 |
| TL1250F180BQRCLR | SPST - Tactile Switch N.O with Blue Led | 2 | SW1-2 |

3. Place the components on the schematic sheet. The schematic is on the next page for reference. Feel free to print the page for this easier viewing.

   Remember that symbols may be mirrored as well as rotated. However for most cases use the appropriate alternate symbol to match the schematic.

   Parts **STP1** is a 2-pin Star point symbol. It resides in the library and has a PCB star point footprint representing a large single pad component. In fact this is special component that allows two nets such as ground returns to be connected together at a predetermined location using routed traces.




The red symbol is created out of figures and grouped together to represent a speaker. The actual speaker for this project is not mounted on the PCB. Only the Solder eye terminals are used.

The block shape shown as **Optional Amplifier** is a Hierarchical Block. This will be covered in a later step.

As you create the schematic, feel free to make adjustments to the;

- scale of the symbols using the Item Properties dialog
- size of the text and fonts using the Assignment settings
- position of the attribute test introduced with the part.
- colours using the Colours dialog.
- local visibility of pin names/identifiers for parts such as resistors and non-polarized devices

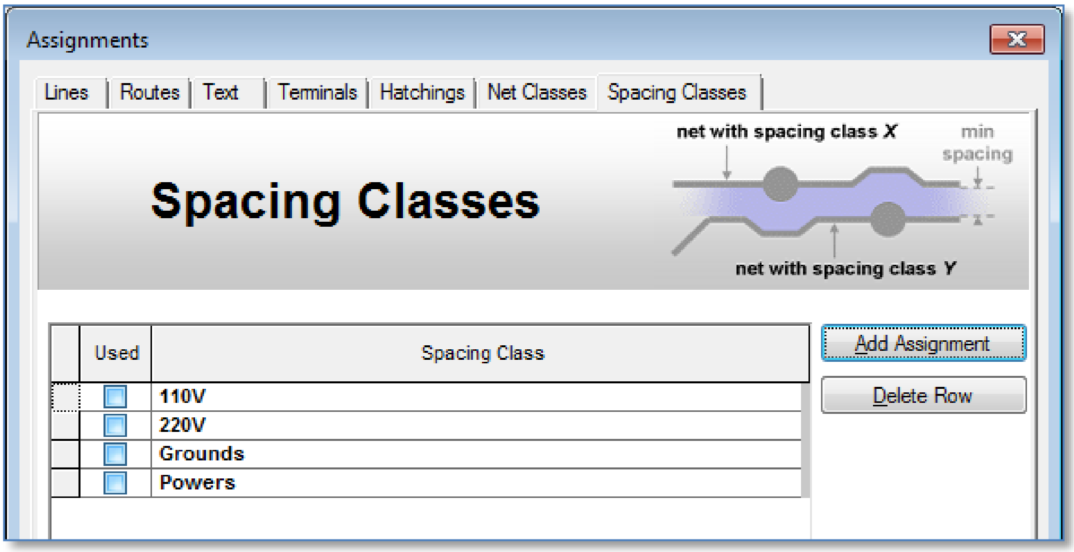
4. Save the design as **Rainmaker1.SCM**

5. Connect the components – Note that the connections are different colours. This is due to the use of different route codes.

| | |
|---|---|
| For Power Nets (red) use | Net Route Code **VCC** |
| For Ground nets (green) use | Net Route Code **GND** |
| For all other nets (purple) use | Net Route Code **Signal** |

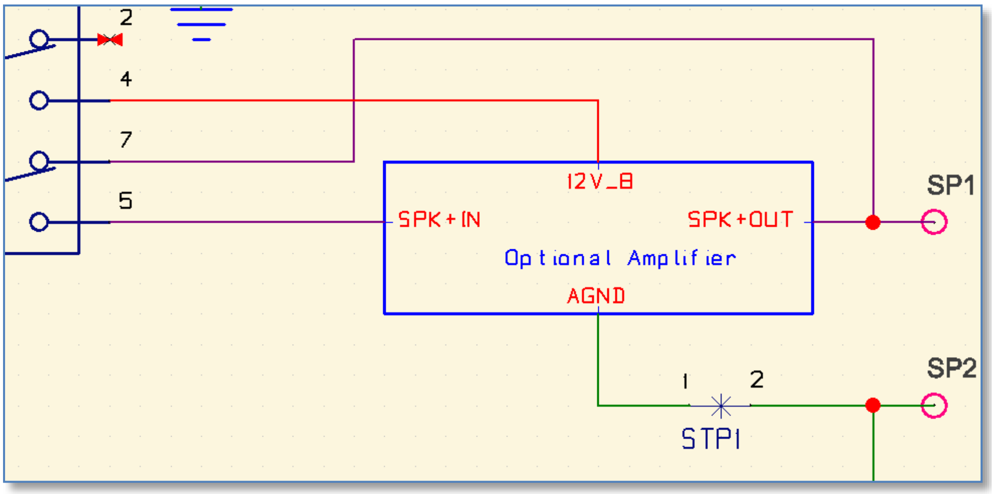
6. Add Global Signal symbols accordingly. They can take on unique net names. See the schematic for the appropriate names.

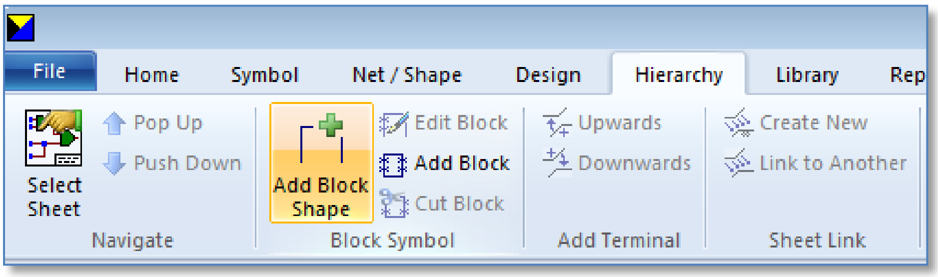
7. Optional step. If you would like to learn about using Spacing classes, you will find it very useful to declare unique spacings between groups of Nets. Circuit designers appreciate being able to define this information in the schematic.




8. Save the design as **Rainmaker2.scm**

We will now add a second sheet to this design. This will be a lower level hierarchical sheet that we can *push down* to and *pop up* from as we move from sheet to sheet. To connect to the sheet we will add a hierarchical block with terminals to emulate signals connected to the lower sheet. The signals names are shown below in red. The block has been named “Optional Amplifier”

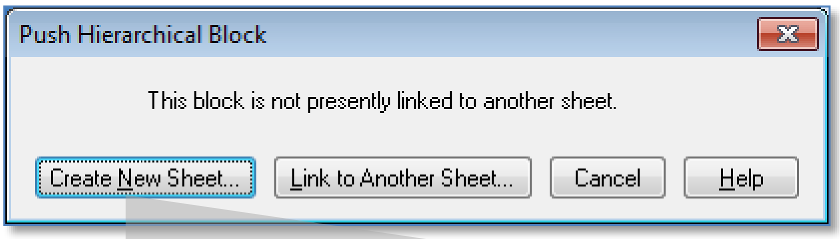



9. From the **[Hierarchy]** tab select **Add Block shape**. Click to start the rectangle start and end position in the approximate location shown in the image above.

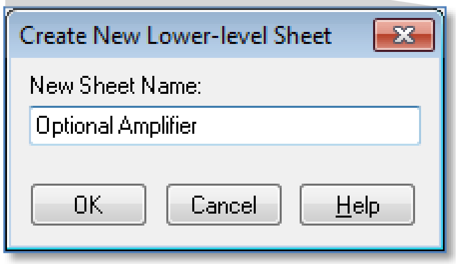
10. Double Click on the block shape outline. You will be prompted as follows.

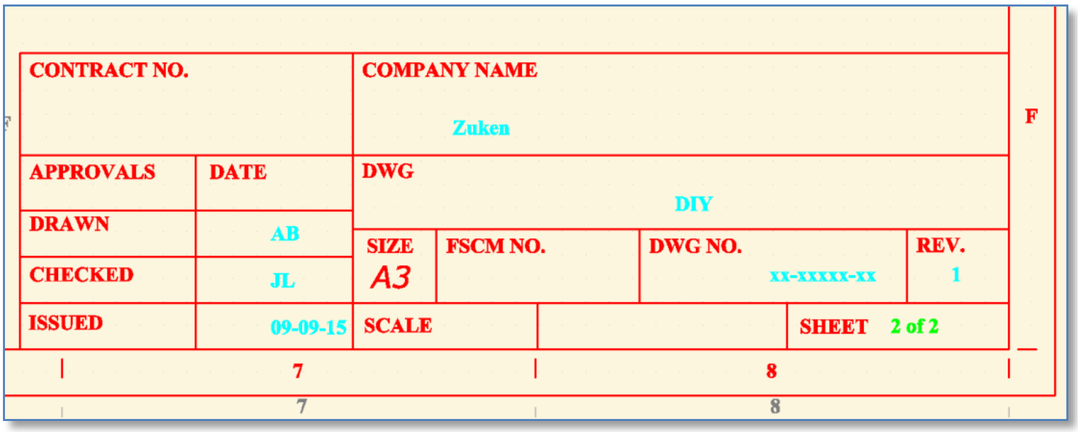
Select **[Create New Sheet]**




Name the new sheet “**Optional Amplifier**”.

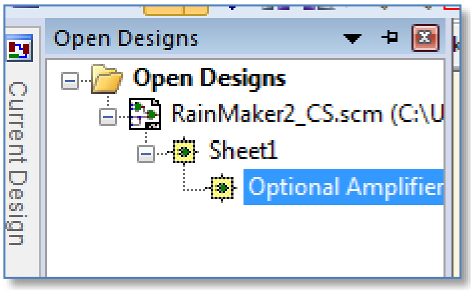
Click **[OK]**





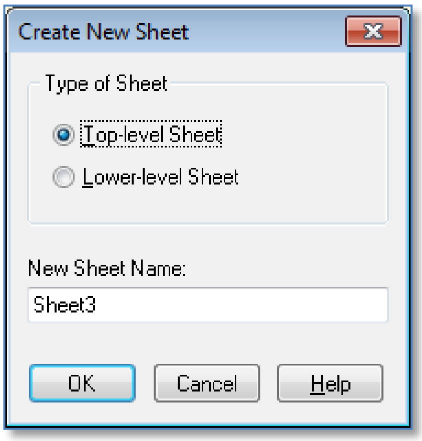

You are now in a new schematic window using the same format sheet symbol labelled Sheet **2 of 2.**

11. Open the **Open Designs** auto-hide panel to see that the new sheet appears indented to suggest that it is a child sheet of the **Sheet1** parent.




**Note:** Here you may rename **Sheet1,** if you wish by clicking on the name and clicking the **<R.M.B.>.** Select **Rename sheet.**

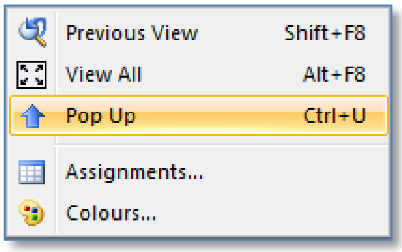
**Note:** New Sheets may be added in this same manner by selecting **Add Sheet.**




Top Level Sheet will be at the same level as sheet 1.

Adding a *Lower-level Sheet* will create it as an *unconnected sheet* and be displayed as a light blue icon. This means that a Hierarchical block will be needed to bring the new child sheet under the desired parent sheet.

12. Click inside of the **Optional Amplifier** sheet space and the click the **<R.M.B>**. Click the Pop up option to take you upwards to the parent sheet.

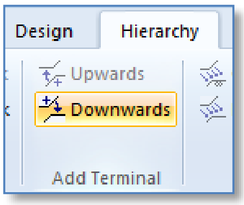



This function as well as **Push Down** or doubling clicking on the hierarchical block shape makes it easy to move from sheet to sheet.

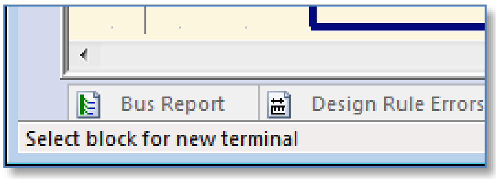
Next we will add terminals to serve as connection points to emulate net connectivity between the sheets.

**Note**: that this is optional as common signal names are automatically merged during the *sheet collating* phase, such as during the transfer to PCB process, ECO update and Back Annotation, etc.

13. Click the **Downwards** option on the **Add Terminal** section of the **[Hierarchy**] tab.




**Note:** Steps are dictated for functions at the lower left corner of the application window.



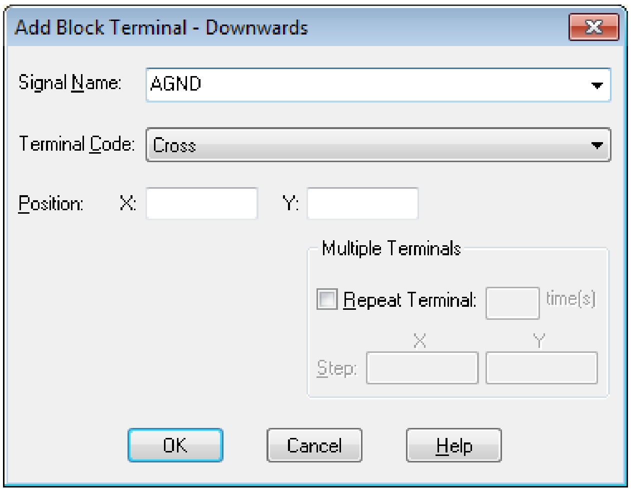

Click on the block shape. From the dialog, open the *Signal Name* list and select **AGND.**

Change the *Terminal Code* to **Cross.** This terminal code uses a 'Plus' shape.

Click [**OK**].

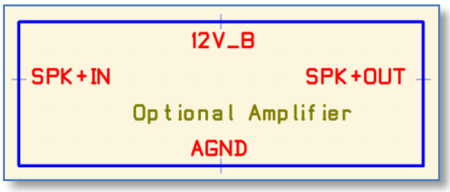
Place the terminal on the bottom side of the block outline as shown.

Press the **<esc>** key on the keyboard or click the **<R.M.B.>** and select **Cancel**. This will return to the dialog.




You may specify new net names as well.

Enter the signal name **12V_B** then click **[Ok]** and position this terminal on the top of the block symbol as shown.

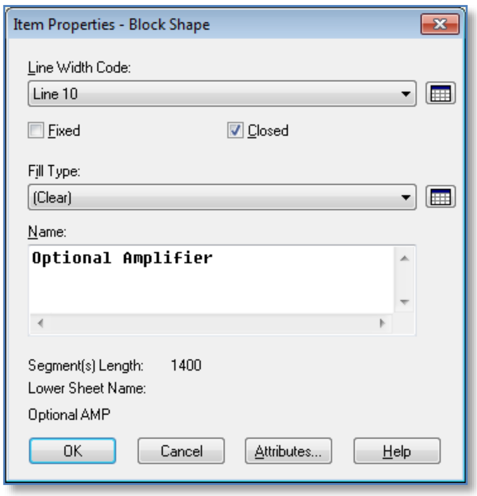



Repeat for **SPK+IN** and **SPK+OUT** placing them as shown.

Click the **<R.M.B.>** and select **Finish.**

You may position the terminal name labels as you like.

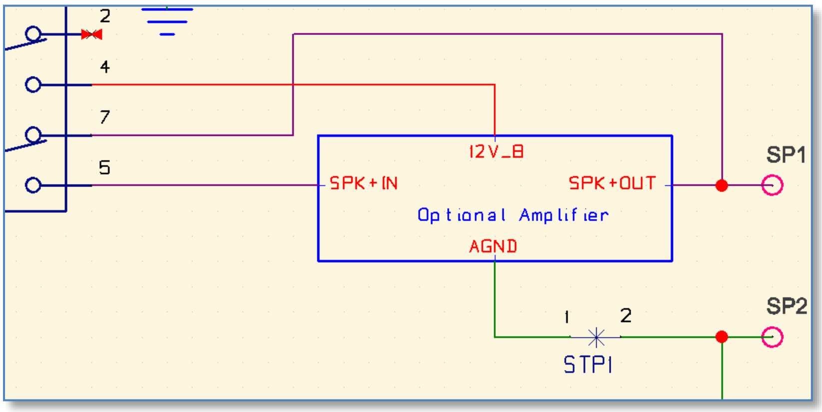
14. To apply a name to the block symbol select the outline and enter **Optional Amplifier** as shown and click **[OK]**.



15. ***Push Down*** to the Optional Amplifier sheet to see the lower level terminals. As each terminal was placed, its corresponding hierarchical terminal was placed at the same X, Y location on the lower sheet.

   **TIP*:*** As the demonstration video shows, Hierarchical terminals codes can be changed, if so desired, using the Item Properties panel. For instance the Hierarchical terminals on the lower level sheet can be assigned a terminal code that represents a filled arrow whereas the Upper hierarchical terminals may continue to use the Cross terminal code.

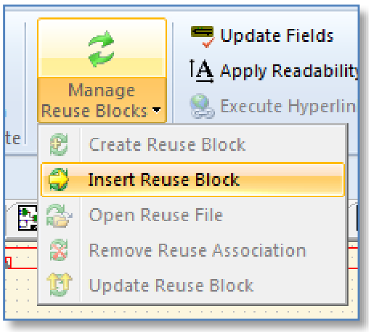
16. ***Pop Up*** to Sheet1 and finish adding the connections to the new hierarchical terminals as shown on the schematic. Remember to set the Route Codes to maintain the same colour correlation.




17. Save the design as **Rainmaker3.scm.**

We are now ready to add the reusable circuit block that we saved in chapter 1.

Creating lower level circuit blocks for the purpose of adding reuse blocks is a nice way to maintain a tidy design flow, though they are not required.




18. ***Push Down*** into the lower level sheet.

19. From the **[Design]** tab select **Manage Reuse Blocks → Insert reuse Block.**

   Select the Amplifier schematic block.

   As the block is integrated into the main design items such as component reference designators and net names are checked and compared to those already used.

   Duplicate component names are renamed to the next available reference designator per their prefix stem name.

   Duplicate Net names are prompted with the adjacent dialog allowing the user to decide to *Join* the nets or *Rename* them to keep them separated.

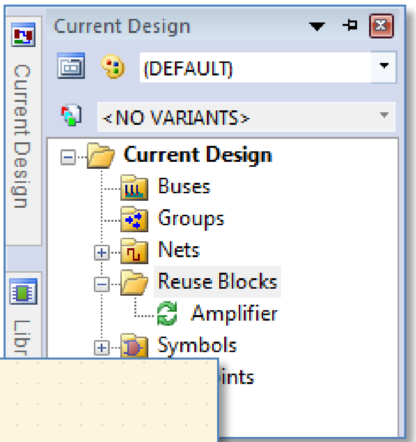
Since you have connected the AGND hierarchical terminal to the starpoint part, the net does in fact exist and we can Join this instance. Click **[Join]**

The following dialogs are very important to consider. If you are familiar with every net name in both circuits and agree that it is ok to repeat the ***Join*** operation for every duplicate net then do so. Else you may cycle through each net individually to avoid joining two nets together accidentally.

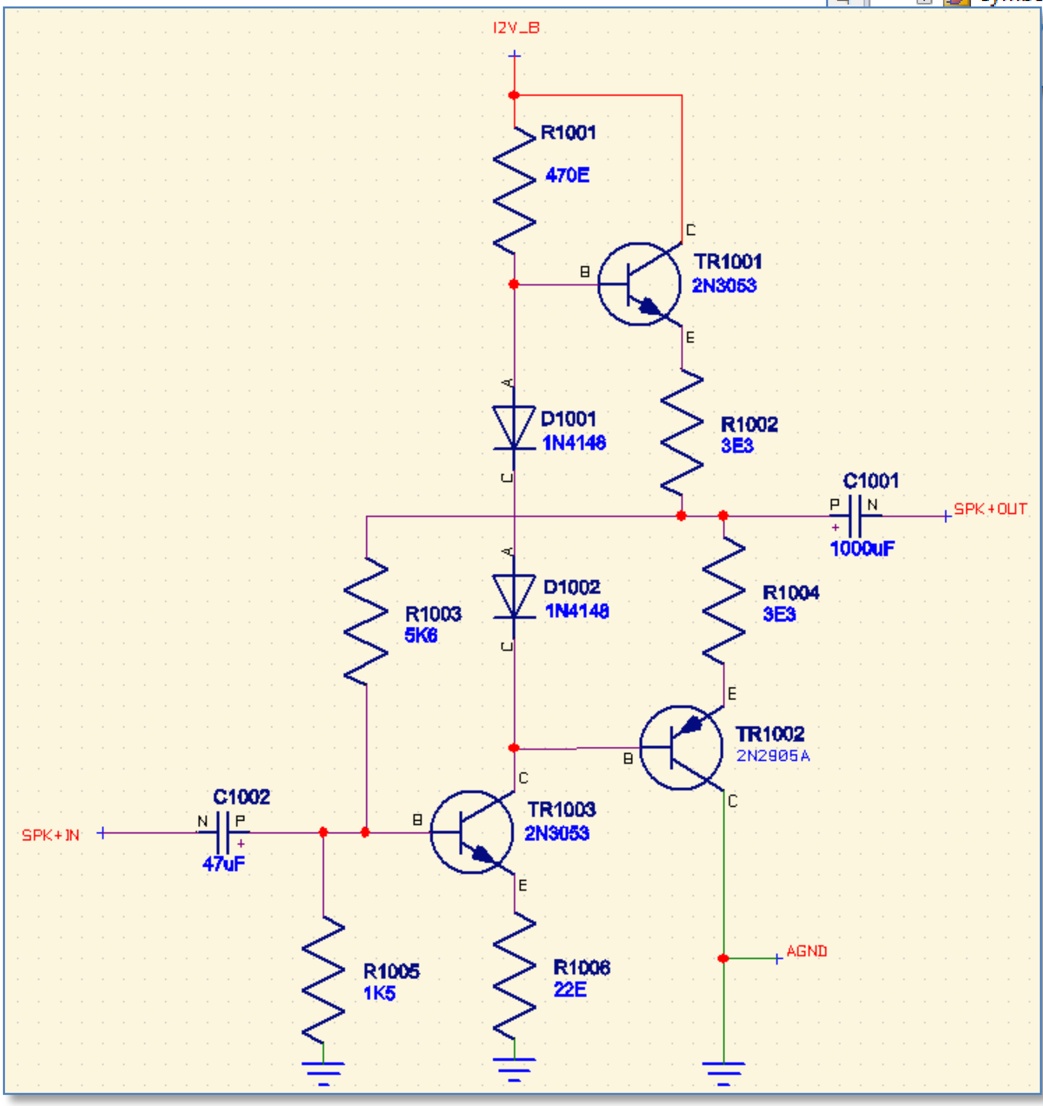
20. The Amplifier circuit is now attached to your cursor. Place it on the sheet.

    The circuit is now grouped and in a state of being locked as a reuse block.

21. Open the Current Design panel menu. Expand the Reuse Blocks branch to see the reuse blocks that are currently in the schematic design.




22. Place the Lower level Hierarchy terminals near their respective nets and connect them accordingly.



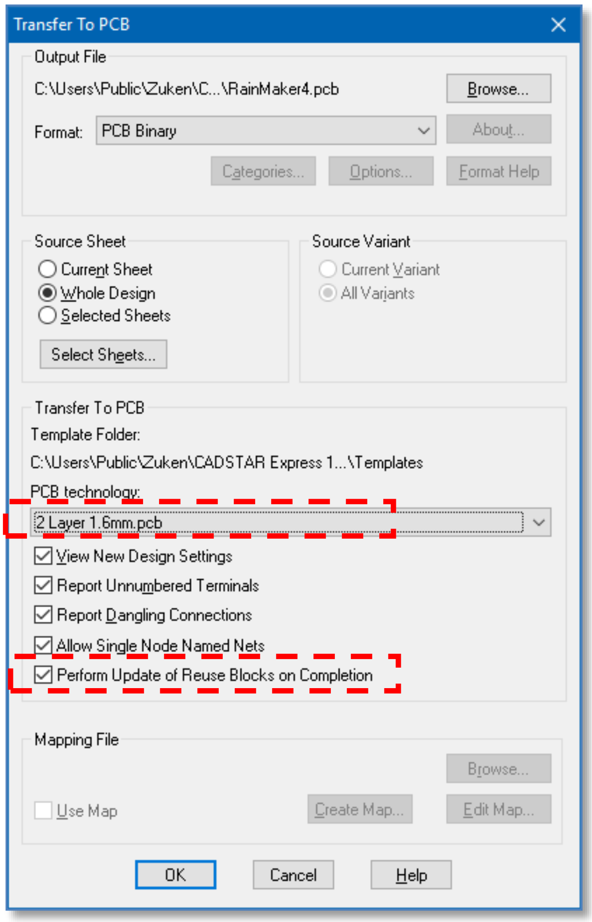
23. Create the Parts List – When prompted select both sheets in the dialog.

24. Print the design.

25. Save the design as **Rainmaker4.SCM**

If you have not completed the design to this point, please load **Rainmaker4_CS.scm** and save it as **Rainmaker4.scm.**

26. Transfer the schematic design to PCB (choose '*2 layer 1.6mm.pcb*' as PCB technology).




Since we are using design reuse blocks you must also check the option (shown below) **Perform Update of Reuse Blocks on Completion.**

You will be presented with several verification dialogs pertaining to new items to add to the design.

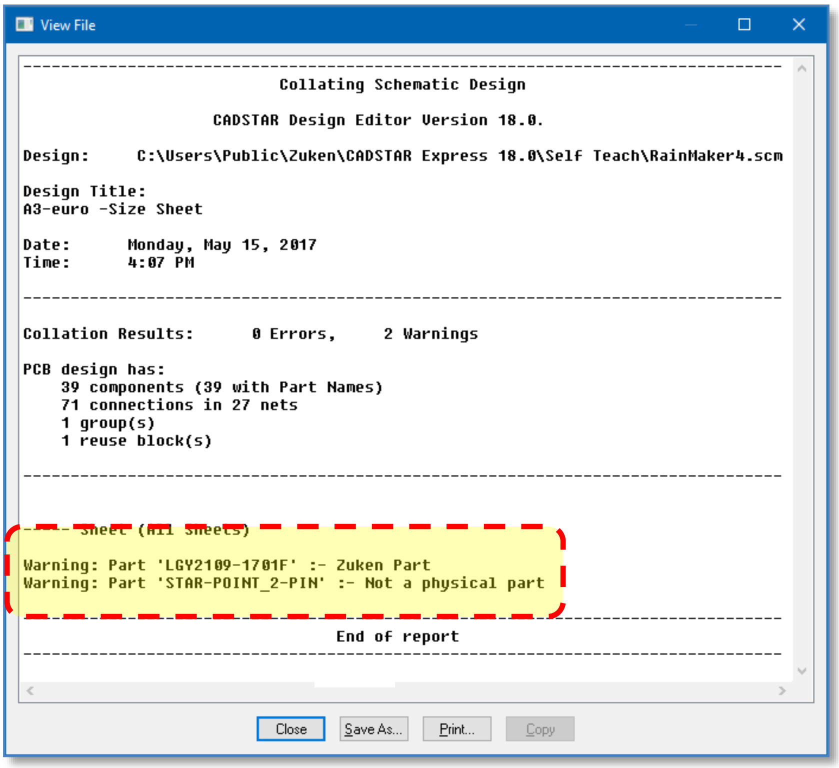
Accept them until the **Reuse Block Update Summary** report appears as shown. →.

**Note:** the warning reflects the use of the *Part Acceptance* attribute used in the parts library definition for;

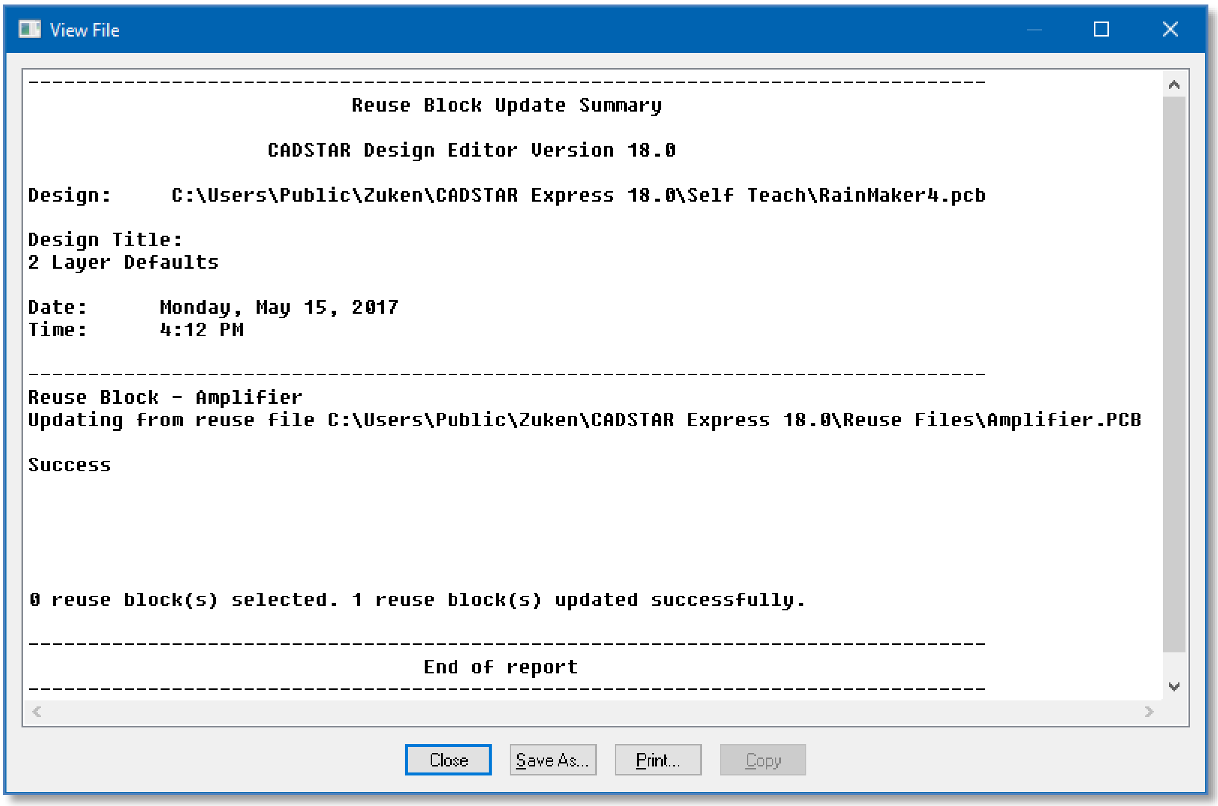
“LGY2109-1701F” and “STAR-POINT_2-PIN”.

For these parts the text string values have been highlighted for this attribute. You will learn more on this in the next chapter.

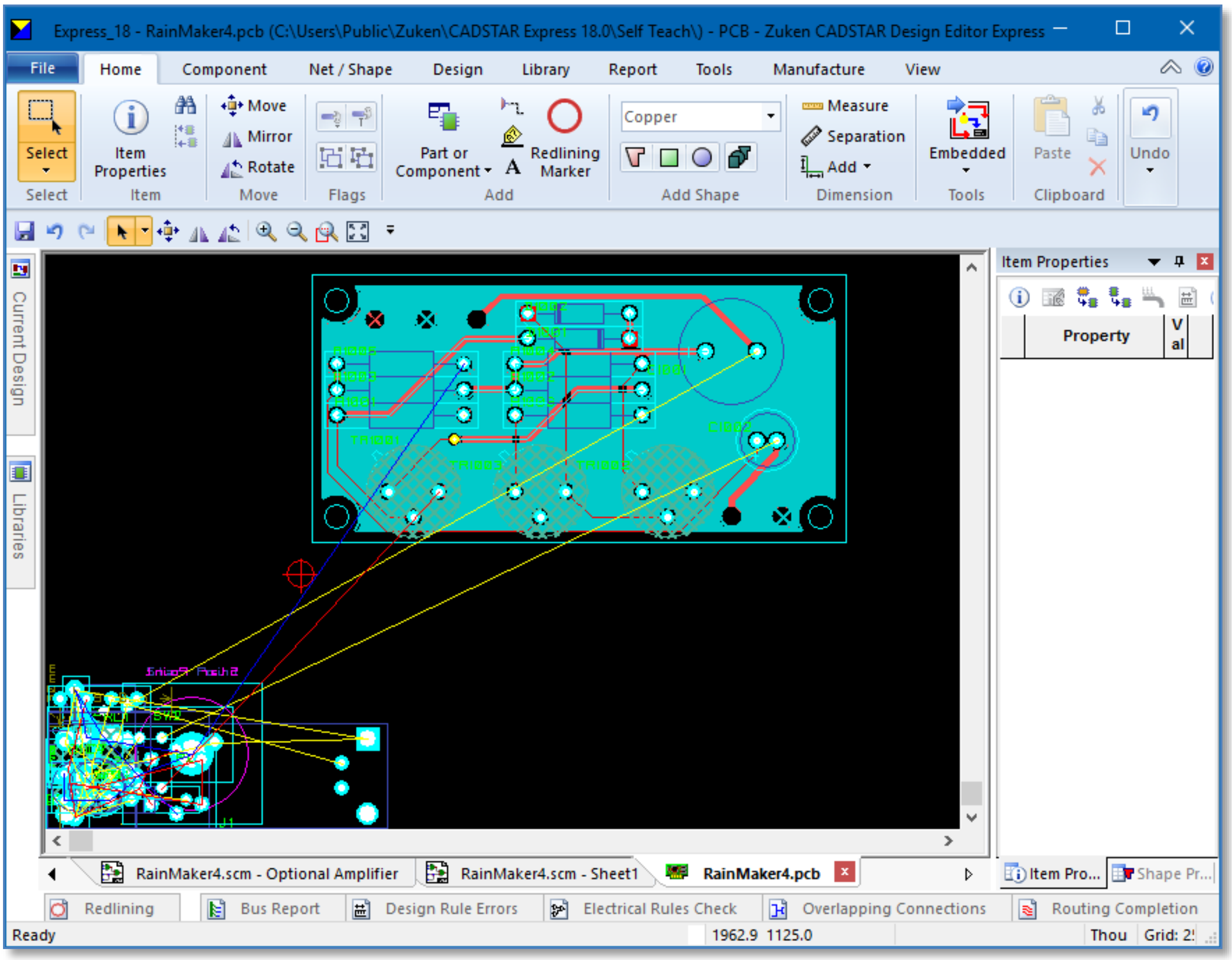
Click [**Close**]



The new PCB design is displayed along with the reuse block, grouped, as shown below.




```
--------------------------------------------------------------------------------
                          Reuse Block Update Summary

                   CADSTAR Design Editor Version 18.0

Design:     C:\Users\Public\Zuken\CADSTAR Express 18.0\Self Teach\RainMaker4.pcb

Design Title:
2 Layer Defaults

Date:      Monday, May 15, 2017
Time:      4:12 PM

--------------------------------------------------------------------------------
Reuse Block - Amplifier
Updating from reuse file C:\Users\Public\Zuken\CADSTAR Express 18.0\Reuse Files\Amplifier.PCB

Success



0 reuse block(s) selected. 1 reuse block(s) updated successfully.

--------------------------------------------------------------------------------
                                End of report
--------------------------------------------------------------------------------
```




**Note**: the reuse block has been moved slightly by the author from its original location for image clarity.

CADSTAR

## Step 2 - PCB Placement for Design B

You can now start to place and arrange the components on the PCB after the transfer. If you have not completed the design to this point, please load **Rainmaker4_CS.PCB,** save it as **Rainmaker4.pcb** and skip to Step 5.

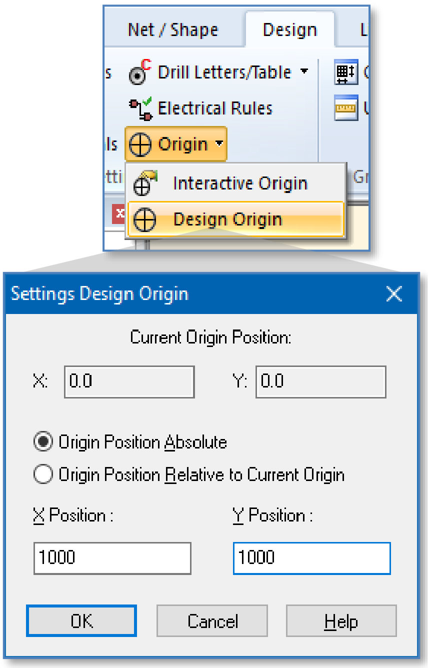
1. Check and/or change the Units & Grid (25 thou is preferred).

2. Click on the Amplifier circuit block and move it to the right of the components to make way for the incoming board outline.

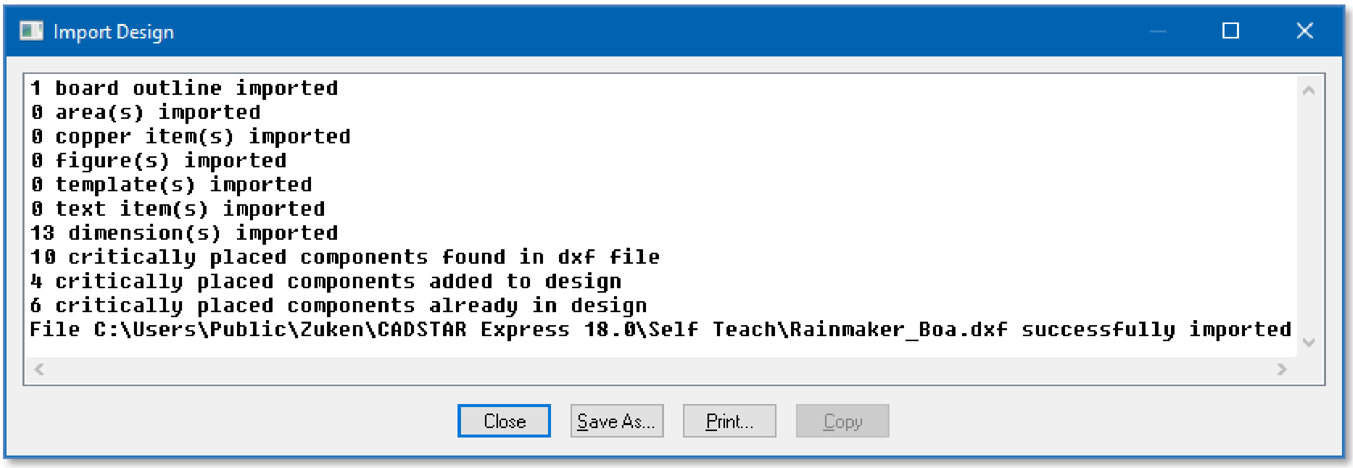
Remember, when a new PCB design is created all components are placed in the positive quadrant of 0X, 0Y, this is considered the initial Design origin.

3. Select the [**Design**] tab and click on [**Origin→Design Origin**].

   You will see the design origin symbol move to X 1000, Y 1000.

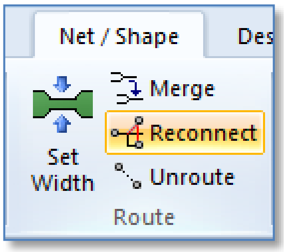


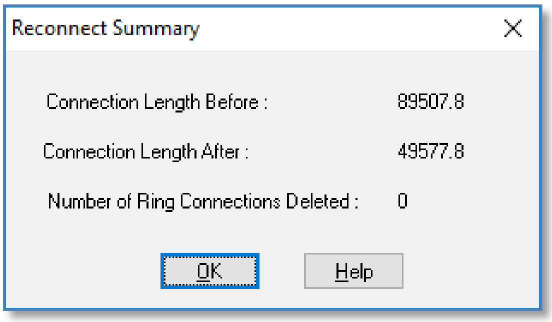

4. Import the DXF Board outline using the **Rainmaker_Boa.dxf** file located in the **\Self Teach** folder. Also use the same **dxfin.map** file. This DXF file also contains other information such as Critical Component placement and dimensions as if provided from the mechanical engineer.

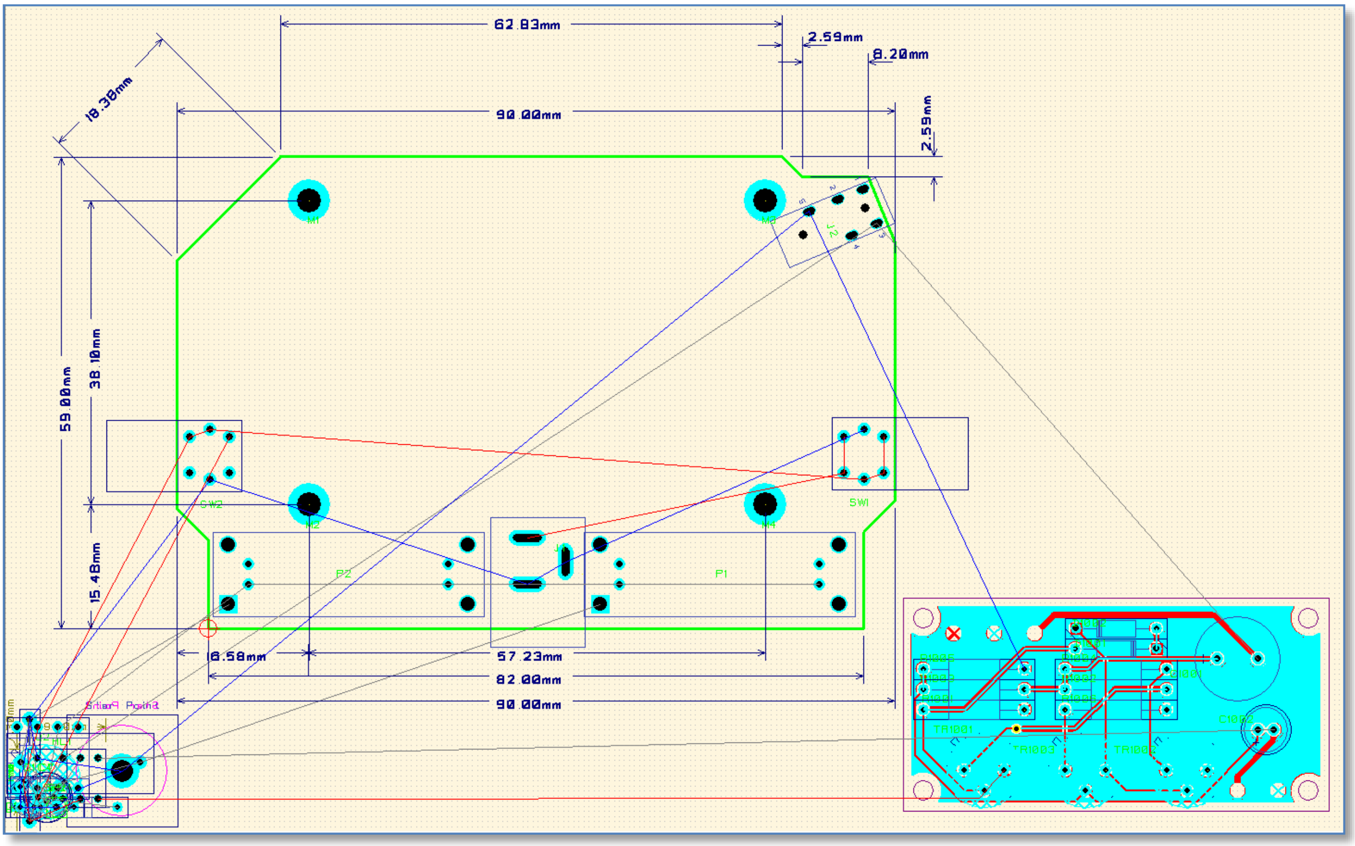



**Note:** From the image above, 4 critically placed components have been added to the design. This refers to 4 mounting holes that are imported as single pad components. The DXF Import process will acknowledge the ref des and component reference shape request. If it is not in the design, CADSTAR will import it from the Parts library. This process is described fully in the CADSTAR Help.

**Tip:** Once the PCB window displays all of the information from the DXF file, you may find that the connections are not optimized (to their shortest length). This can be quickly resolved using the **Reconnect** feature located on the **[Net/Shape]** tab. This function will simply optimize the appearance of the connections thus eliminating length. This does not have any impact on the Signal integrity constraints.




**Note:** PCB design shown after reconnect function has been run.
**Note**: the reuse block has been moved slightly by the author from its original location for image clarity.

If you have not completed the design to this point, please load **Rainmaker5_CS.PCB,** save it as **Rainmaker5.pcb.**

Next we can move the reuse circuit block into position. Since the block is grouped. It is possible to click on it and move it as a single object. It may also be rotated on any angle.

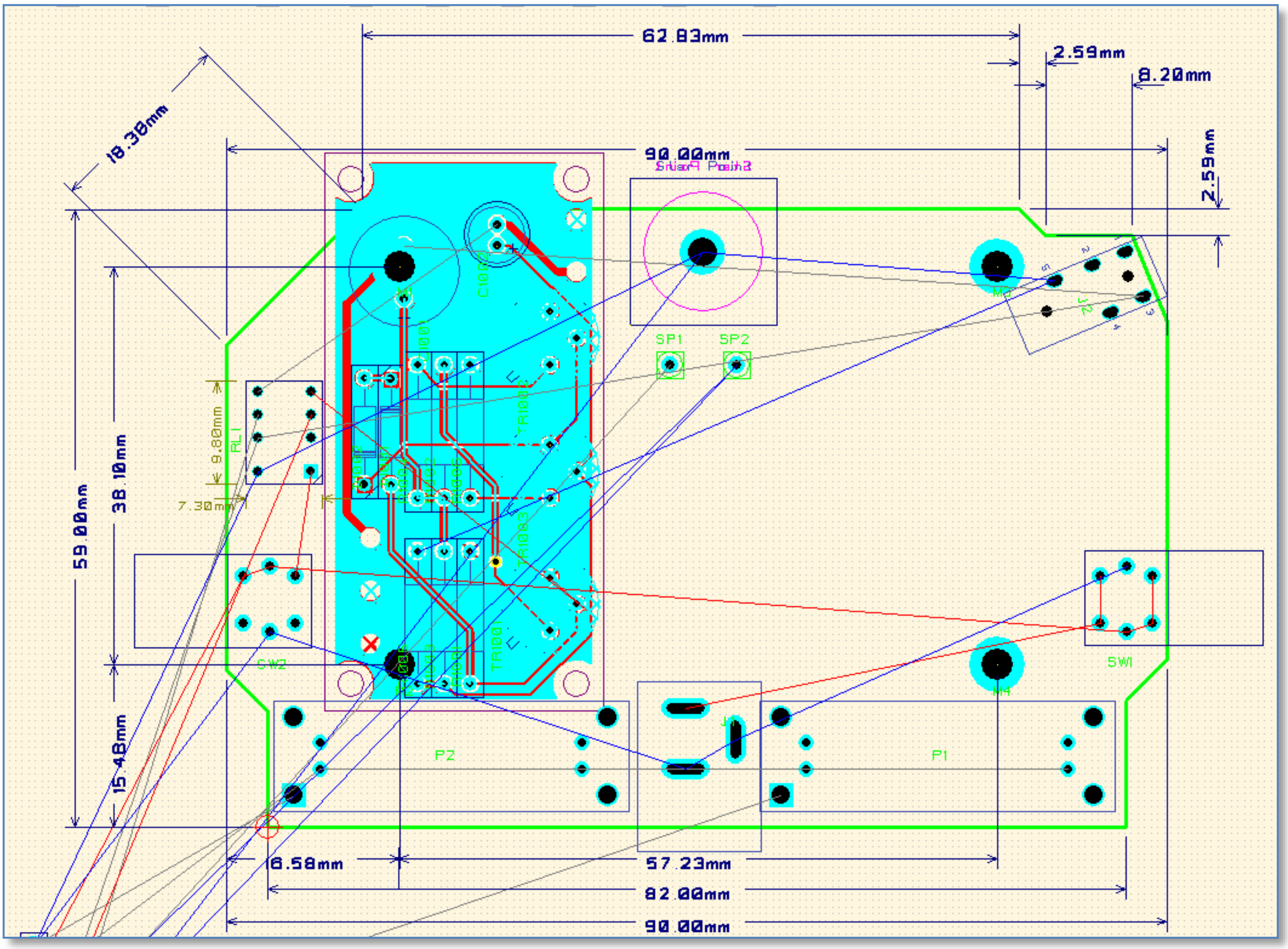
Even though the amplifier reuse block does not quite fit. This is OK and probably a normal occurrence for the experienced PCB designer. Later we will remove the reuse block association make some placement adjustments and *copper pour* template adjustments. The point of the exercise is basic Design Reuse techniques.

5. Place the block as shown below.

   **Tip**: if you pick an object by a location that you would like to change while in the "Move" mode, click the <**R.M.B**.> and select the "**Change Selection Origin**". This will temporarily suspend the movement while you select a different location. Once you click the object the movement will resume.

   **Tip:** Enable the Snap point function located on the [**Design**] tab before changing a selection origin.

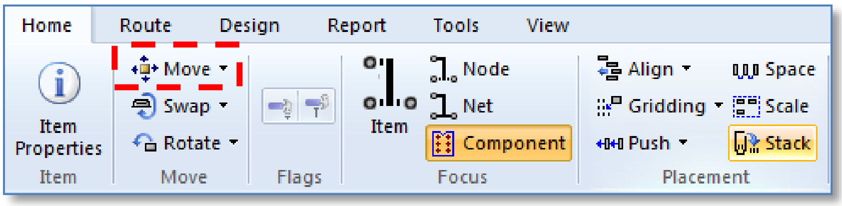
6. Place the Starpoint **STP1**, relay **RL1** and the **SP1** and **SP2** components in the suggested approximate locations shown on the next page. **Fix** them once they are placed by selecting them and clicking **<R.M.B.>** and clicking on the **Fix** function.



7. Select the **Embedded Place and Route** icon located on the [**Tools**] tab.

8. Arrange the components around the board outline using the **Stack** function located on the **[Home]** tab.

9. Select the **Move** icon and the **Component mode** focus icon and manually place the other components.




10. Exit the Embedded Place and Route and save the PCB Design.

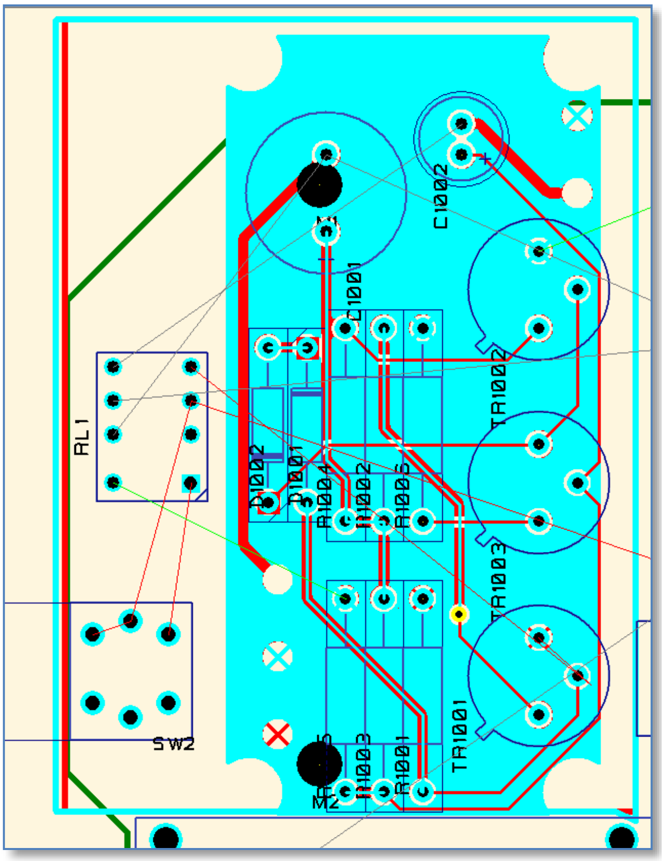
### Adjusting the Reuse Circuit block.

At this point we will make the necessary adjustments to the circuit block so that it fits with this board outline.

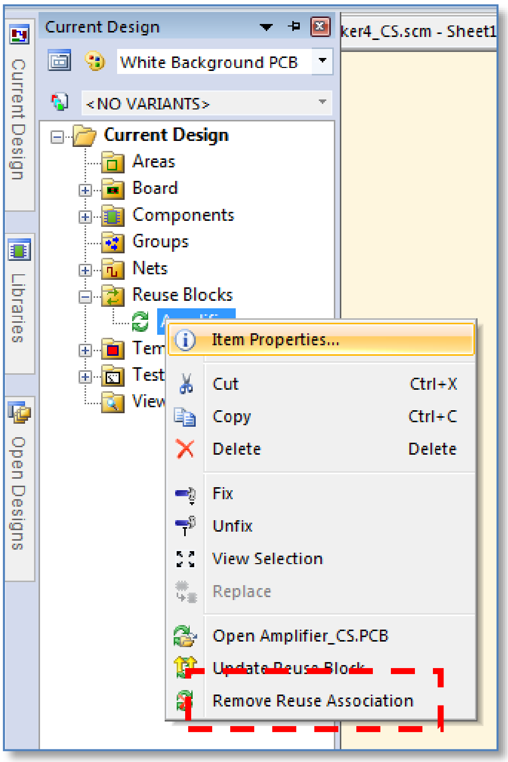
11. Select the Amplifier reuse block. From the non-modal Item properties panel, turn off the Grouped setting.

12. Start by modifying the shapes of the existing copper pour templates that are a part of the reuse block. They can be selected and stretched to the left of the board outline as shown in the image. →

13. Delete the round cut-outs that in the templates. There are 8 total, 4 on each template.



14. Open the **Current Design** panel on the left side of the application window. Expand the Reuse Block branch, click on the Amplifier name and click the <**R.M.B.**>. Select **Remove Reuse Association.** You are now free to make any edits to the circuit block you wish.




**Note:** This is an optional process, it is not necessary to remove the association. If a PCB design warrants this technique, it is recommended to also remove the reuse association in the schematic reuse block as well.

However if you pay attention to the intricacies of the block and later **remote select** the PCB block items from the Schematic window using Cross probing, you can create a new reuse block of the same name to insure that it remains in synch with the schematic.

15. Select the copper polygons and associated templates and delete them from both Top and Bottom layers.

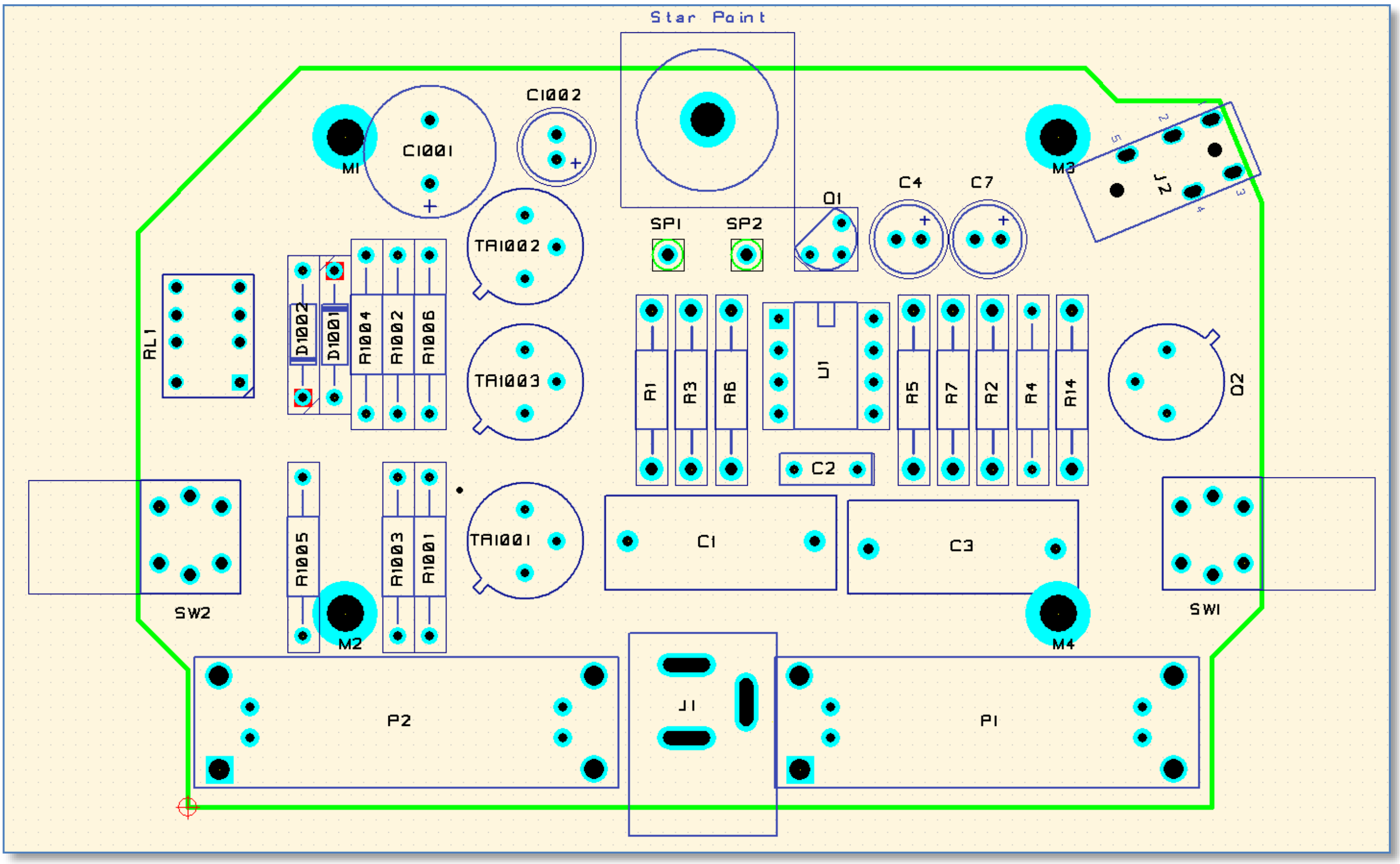
16. Select the **Embedded Place and Route** icon located on the [**Tools**] tab.

17. Use the move commands in the **Component** focus mode to adjust the placement of the two capacitors and perhaps **R1005** to a more proper location.

    If you encounter any errors that you wish to ignore, click the **<R.M.B.>** and select **Toggle errors allowed.**

    As you move routed components, the routes should remain routed as they move with them. .

18. Exit the Embedded Place and Route and save the PCB Design.

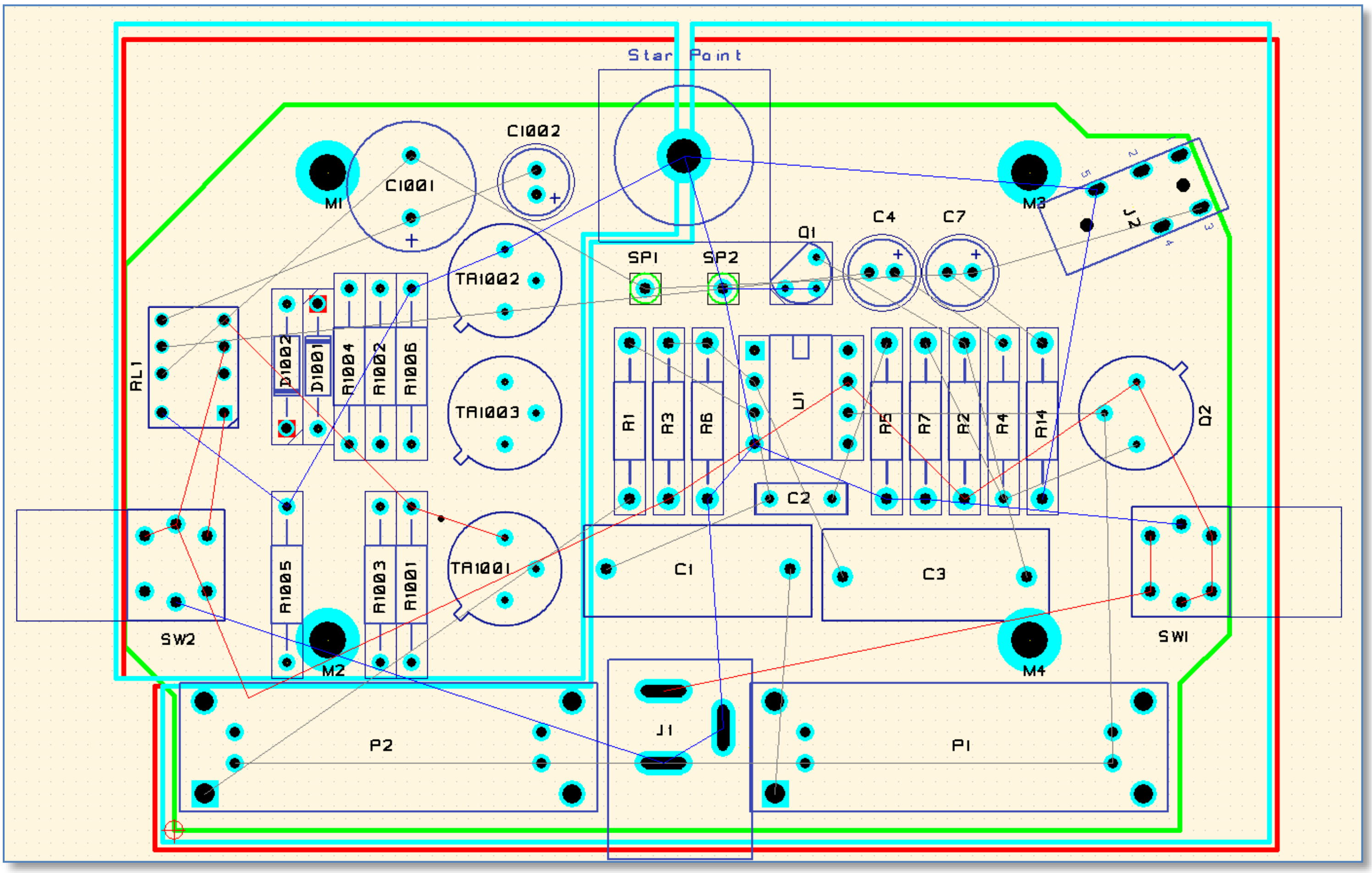



Sample of finished Placement

If you didn't manage to place the components, just open **Rainmaker6_CS.PCB** and save it as **Rainmaker6.pcb.** This file has the copper and templates already removed.

19. Create four new templates to support the power and ground nets from the main Rainmaker circuit. The GND and AGND templates will be on layer *Top Elec*, the 12V and 12V_B templates will be on layer Bottom Elec. Using the Item properties use your judgment when making the settings to the templates.

    Shown below is a suggestion of the shapes for the templates. Those in green represent AGND and GND. The red represent the signals 12V and 12V_B. Notice that the templates can be outside of the board outline. The Copper pour function will only pour up to the board outline minus the Copper to Profile spacing that is allowed.



## Step 3 - PCB Routing for Design B

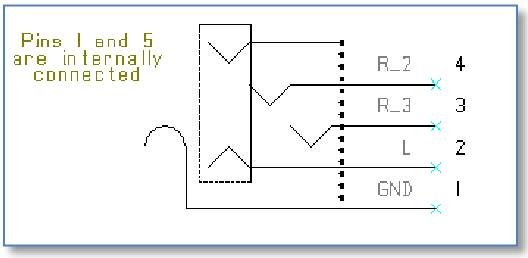
You are now at the final stages of the PCB design. For this task you may use the Fix command to lock the existing routing from the Amplifier reuse block in place.

1. Select the **Embedded Place and Route** icon located on the [**Tools**] tab.

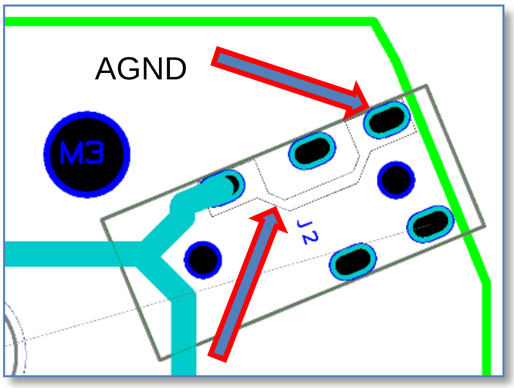
2. Manually route any critical nets such as 12V from SW2 (Shown below as partially routed to the closest 12V template contact point), 12V_relay_enable and 12VA.

3. An additional route (AGND) can be routed on the Top Elec layer from J2 pin 1 or from J2 pin 5 to the Star Point. You can also route from R14 pin 2 to J2 pin 1 or pin 5 as shown in the image below.

   If you recall from the schematic part entry, the symbol indicated that pins 1 and 5 are internally connected. Therefore you did not connect pin 5 to pin 1 using a physical connection in the schematic. These are connected on layer Interconnect, which must be made visible to see.

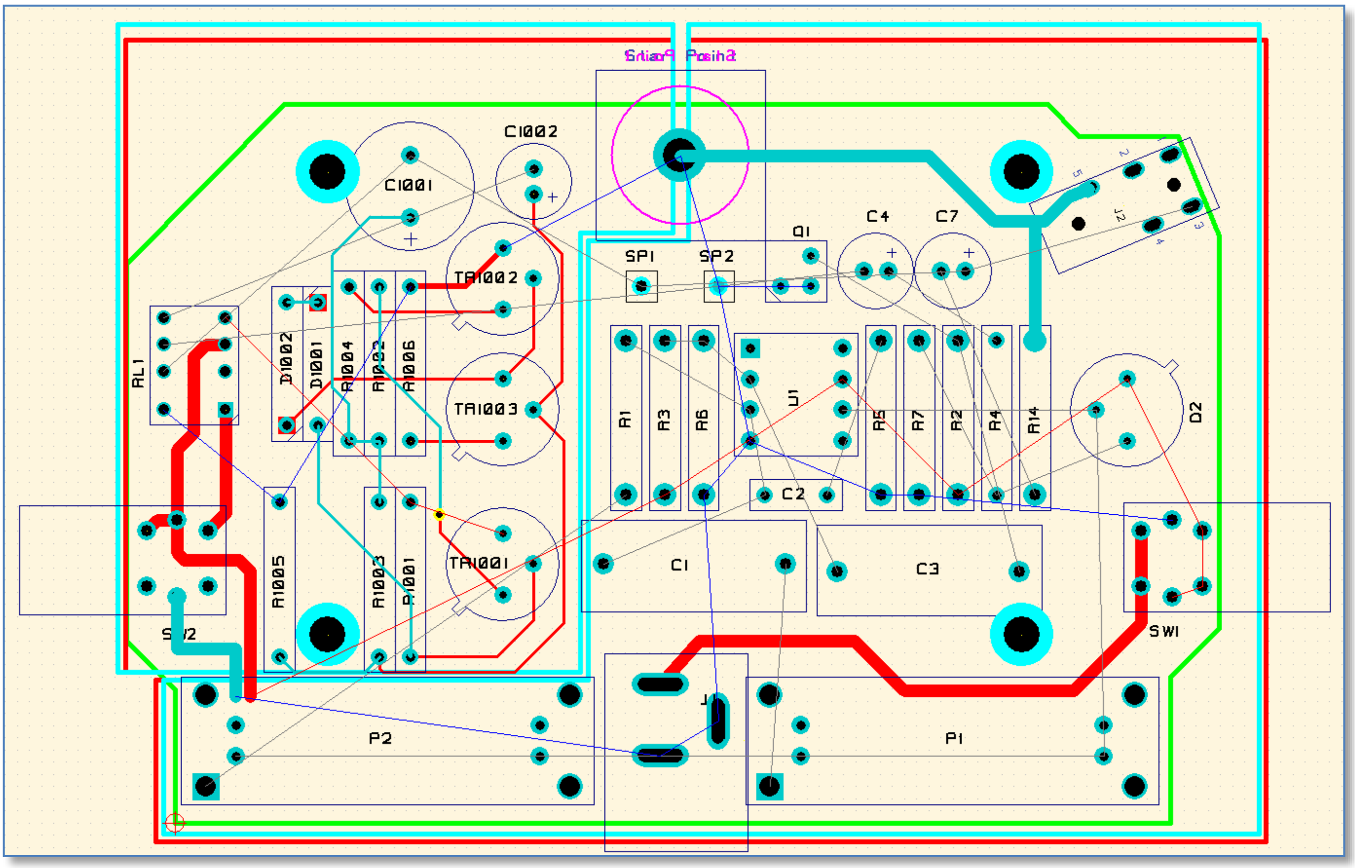



   Perhaps you have encountered some parts where a similar situation can occur. This unique situation can be addressed by creating a closed polygon shape within the component reference shape. This can be drawn on an electrical layer and used as part of the actual copper routing pattern or it can be drawn on a non-electrical layer where the net connectivity is simply implied.




   Once you have routed this pattern, use the **item Properties** function to verify that the other pad is in fact connected to AGND.

4. Using a framing technique, draw a rectangle around the extremities of the PCB outline to select all items. Click the **Fix** command located on the [**Home**] tab.




5. Automatically route all other nets then spend some time manually routing using the Activ-45 routing mode. This is accessible from the <**R.M.B.**> menu.

   **Note:** Do not route any other pins connected to the 4 power and ground nets. This will be completed in the next step.

6. Once you are satisfied with the routing results use the Pour copper function to complete the PCB design. This will make the connections to the 4 power and ground nets.

   **Note:** the two connections coming from the Star point must be routed partially to the finished Copper pour shapes.

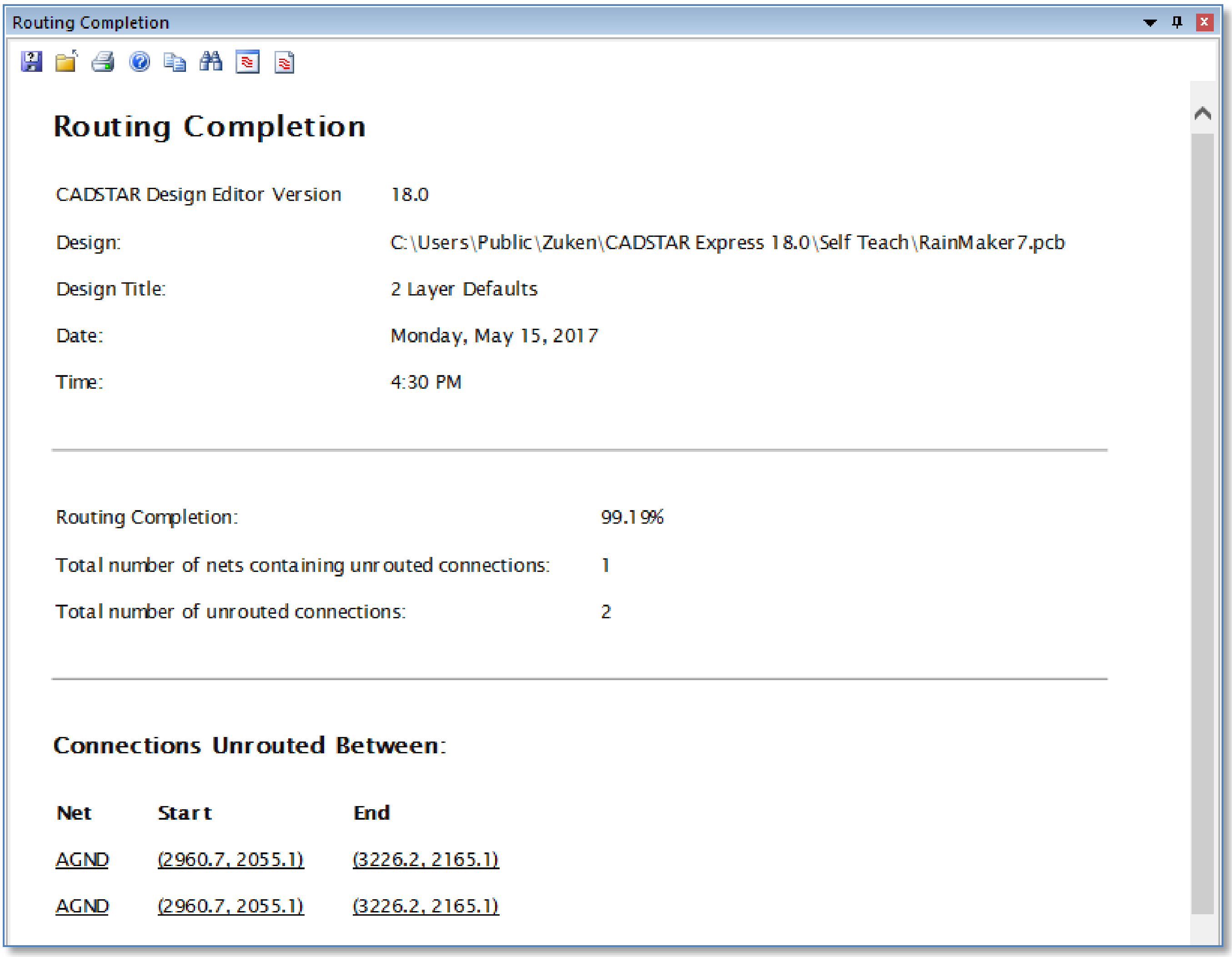
If you wish to fine tune your routing to ensure each power and ground is properly connected to the poured copper, simply ***Undo*** the copper pours or use the **Clear** function.

7. Exit Embedded Place and Route and save the PCB design.

If you didn't manage to complete the design, just open **Rainmaker7_CS.pcb** to have a look.

**Tip:** If you still see connection guides on the power and ground nets, verify the completion of the routing to the copper polygons by generating a **HTML Routing Completion Report**. This is located at the bottom of the application window. A sample is shown on the next page though yours may be different.  Simply click on the Items to see what is being reported.

CADSTAR


Routing Completion

## Routing Completion

| | |
|---|---|
| CADSTAR Design Editor Version | 18.0 |
| Design: | C:\Users\Public\Zuken\CADSTAR Express 18.0\Self Teach\RainMaker7.pcb |
| Design Title: | 2 Layer Defaults |
| Date: | Monday, May 15, 2017 |
| Time: | 4:30 PM |

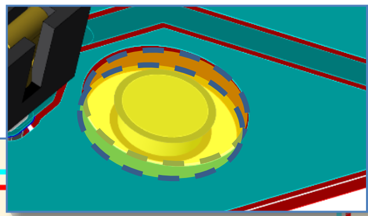
| | |
|---|---|
| Routing Completion: | 99.19% |
| Total number of nets containing unrouted connections: | 1 |
| Total number of unrouted connections: | 2 |

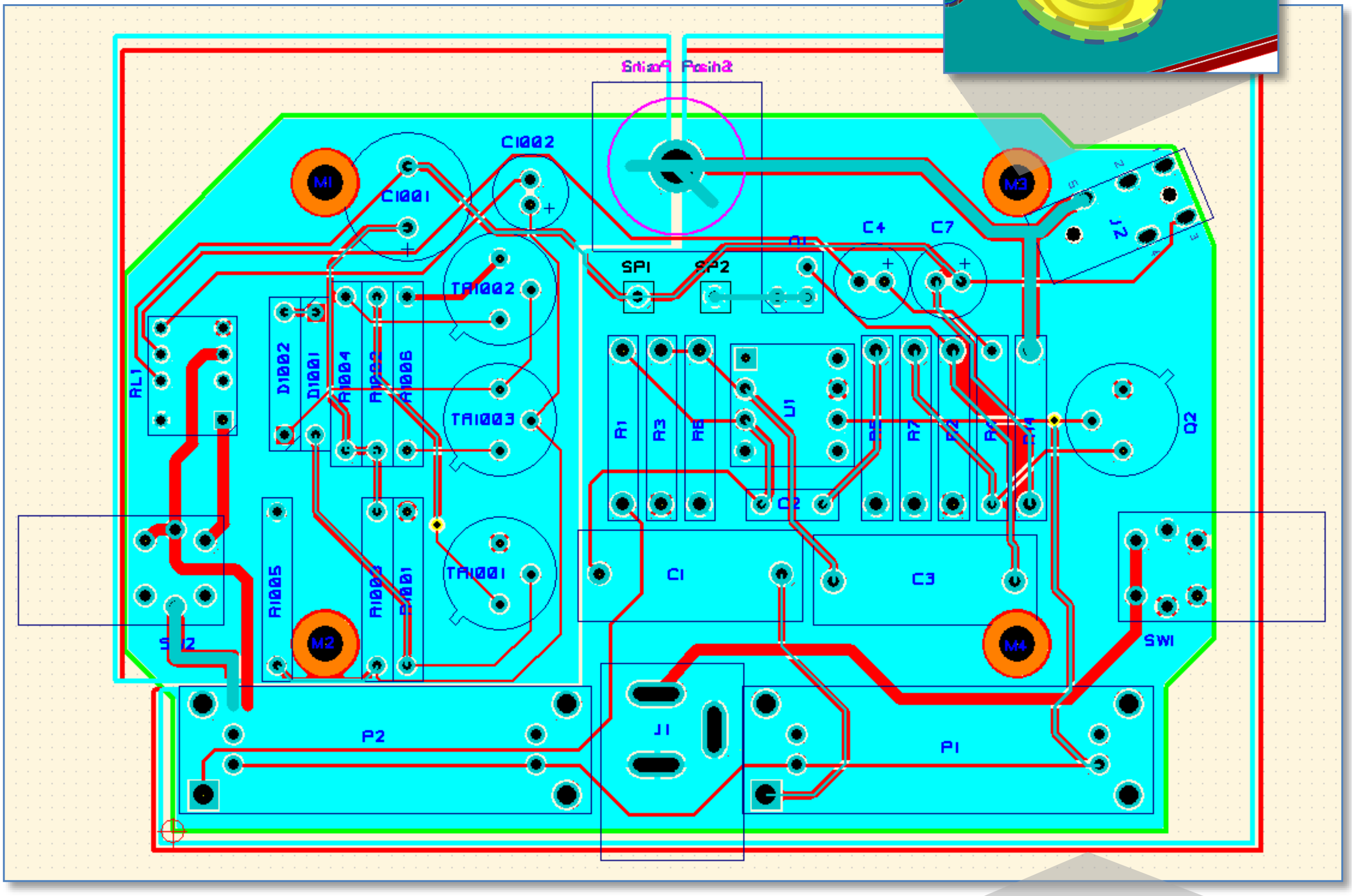
### Connections Unrouted Between:

| Net | Start | End |
|---|---|---|
| AGND | (2960.7, 2055.1) | (3226.2, 2165.1) |
| AGND | (2960.7, 2055.1) | (3226.2, 2165.1) |

Shown below is a sample of the placed, routed PCB with copper poured. RainMaker7_CS.pcb

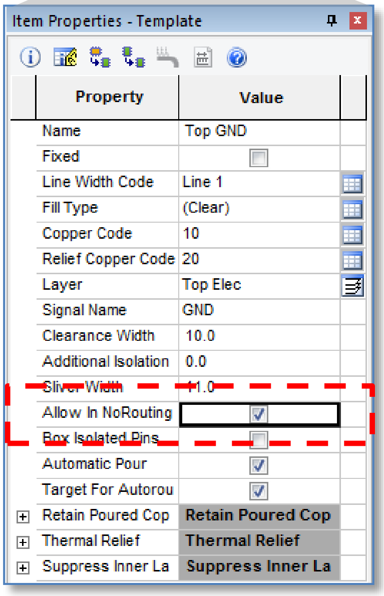
The mounting hole M3 is shown in 3D using **Board Modeler Lite** to illustrate how additional spacings can be applied using items such as ***Keep-out areas*** within the components reference shapes.





A benefit of creating Keep-out areas in the component shapes is they can be enabled within the template properties. →

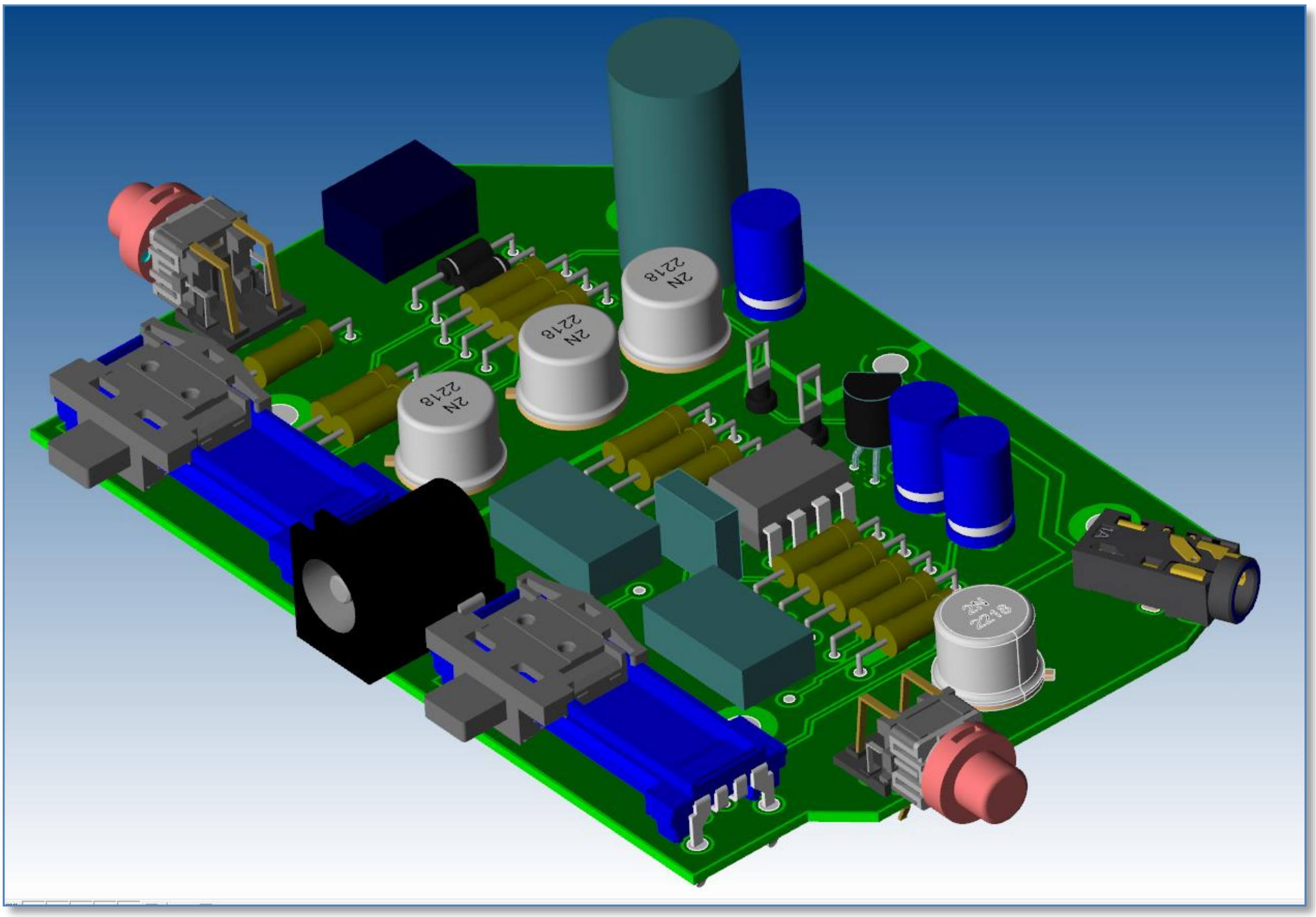
If you experiment with this design, try changing the template property for the **Top GND** to ***Allow in NonRouting*** area. Then use the Embedded Place and Route tools, to re-pour the copper.



## Step 4 - Manufacturing Data for Design B

1. You can select [**File]** tab→ **Manufacturing Export**→ **Batch Process** **[Open**] select ***Manufacturing Output 2 Layer.ppf*** ) in the menu bar to create the manufacturing data.

At this point you might want to check out the capabilities of **BoardModeler Lite**. It supports import/export of STEPS AP203, AP214, ACIS STL and IDF formats; providing you an optimized solution for the placement and verification of a PCB Design in its 3D environment. You can replace the board outline, modify component placements, which are smoothly back annotated, import other PCB designs and housings, then build it all together and run a complete collision check.



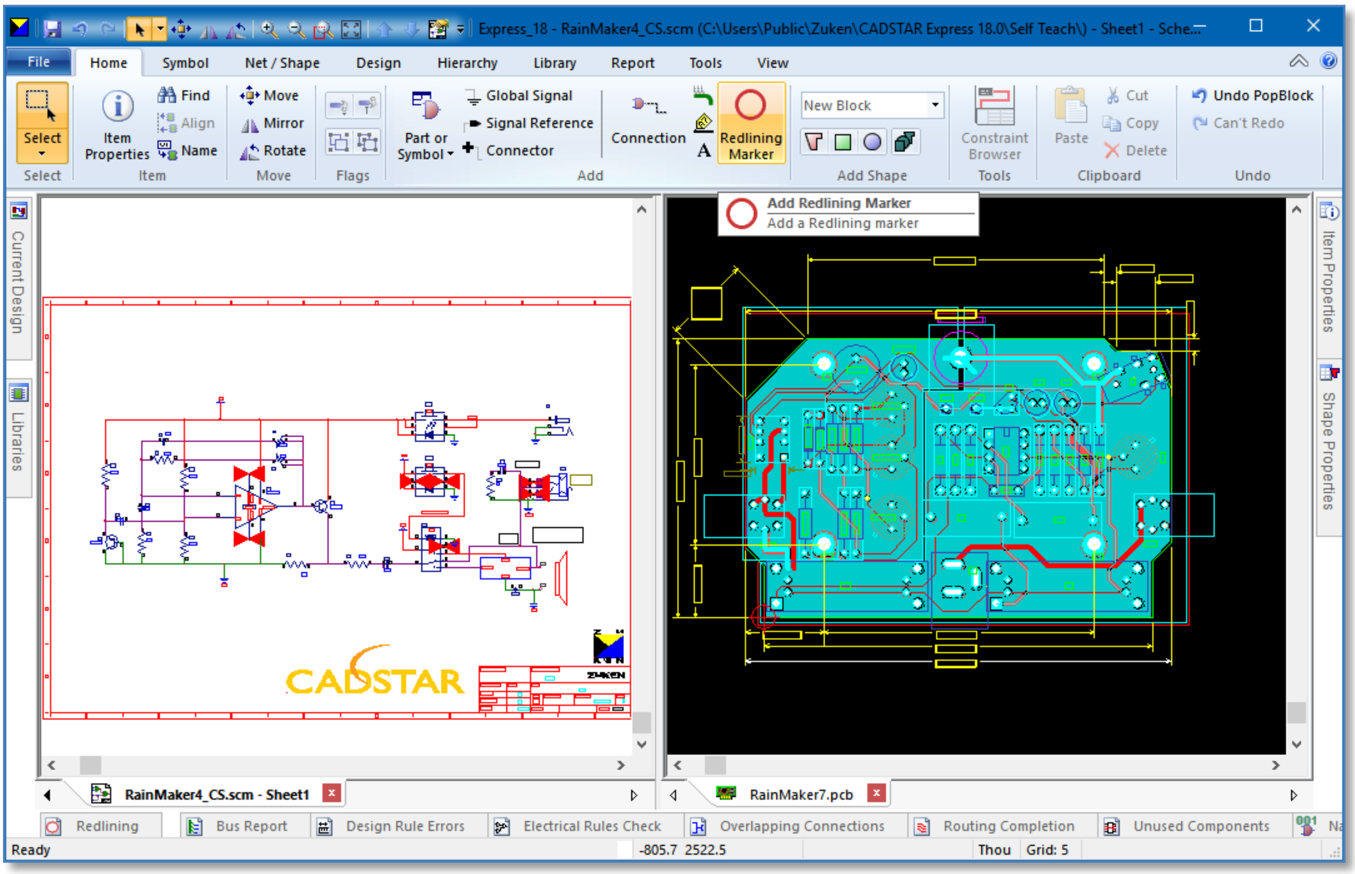
It's not just a viewer!

You can find more information at:

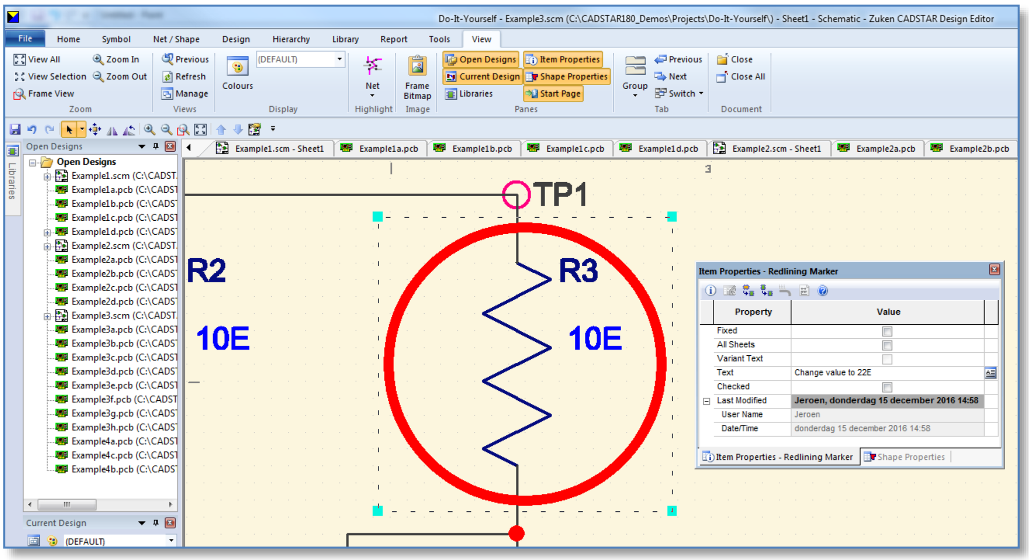
https://www.zuken.com/en/product/cadstar/bundles/

## Reviewing your Designs with Redlining Markers

Another part of the design review process uses a module called “Redlining”. This licensed module is available for purchase with all CADSTAR variants.



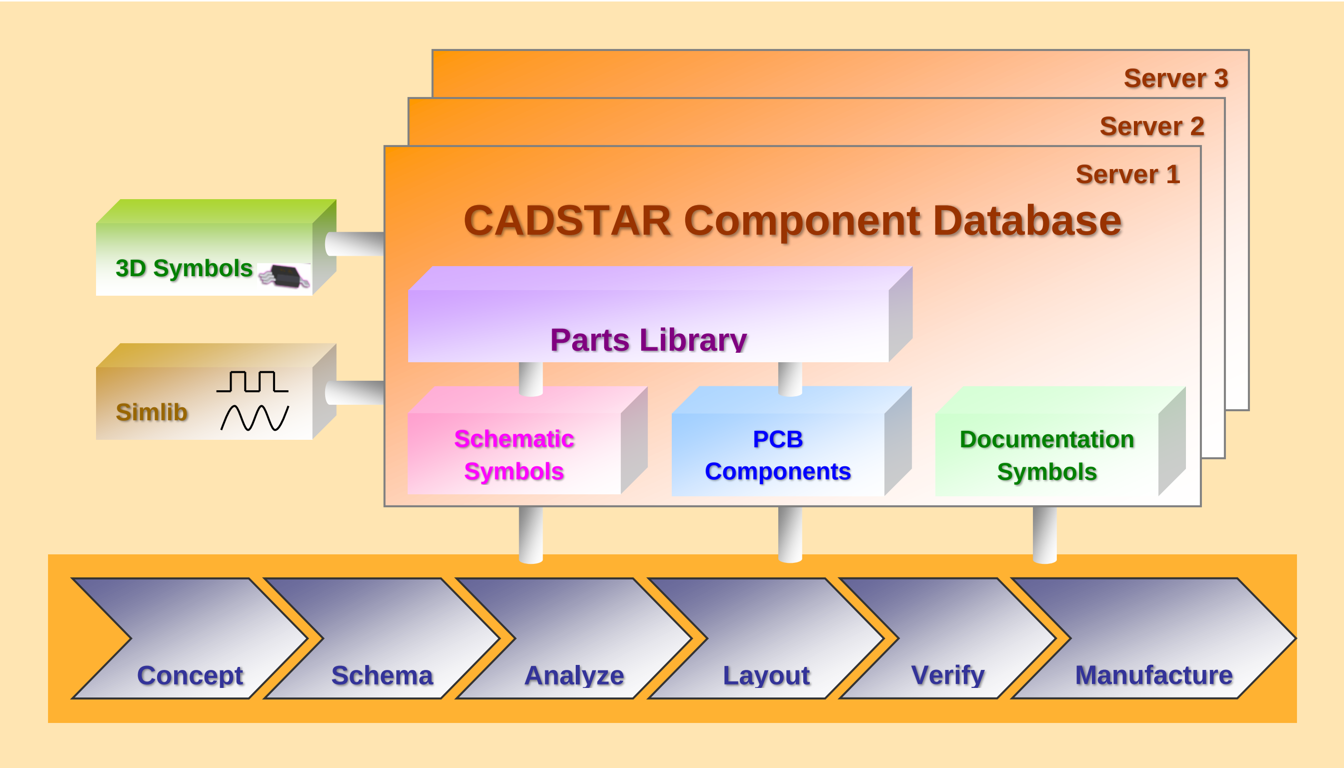

To find out more information click on the [**Redlining Marker**] function located on the [**Home]** tab for a video demonstration. This requires an internet connection.



# Chapter 3 - Library

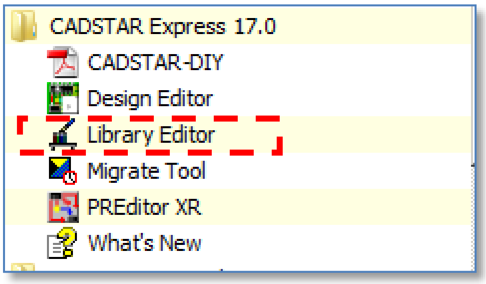
The CADSTAR Library Editor ensures that design integrity is maintained between the symbol, the footprint and the part information, and also supports *multiple* libraries.

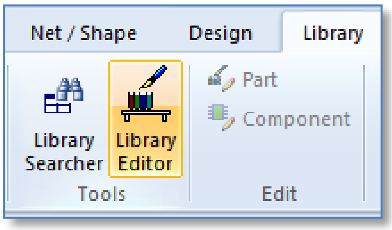
The library provided with CADSTAR Express contains only a few parts essential for the PCB designs described in this ***'Do-It-Yourself Book'*** and some examples of the on-line CADSTAR Libraries. More libraries are available through the ***Zuken Global support*** site. The *ready-to-download-and-use parts* contain all the information you require including manufacturers' part numbers. They are updated and expanded regularly with over ***250,000 parts*** currently available. If the part required is not already available in these libraries, you can quickly and easily design your own parts using the supplied wizards and the Graphical Library Editor. Access to the on-line CADSTAR Libraries is available as part of the maintenance contract.



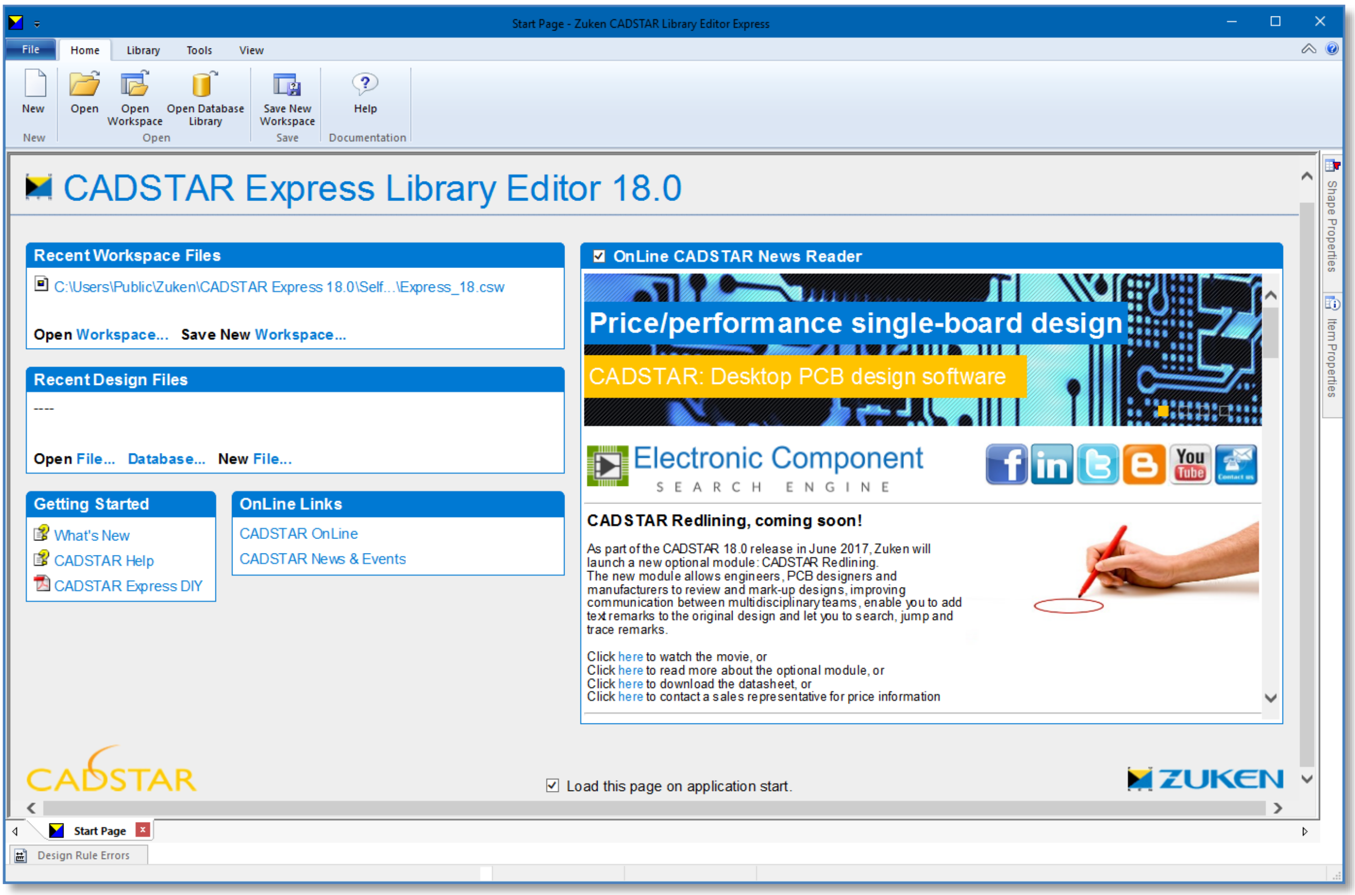
## Step 1 - PCB Component / BGA Wizard

For this next step, we will be using the **Graphical Library Editor**. This can be launched from the Windows Programs menu or from within the Design Editor.



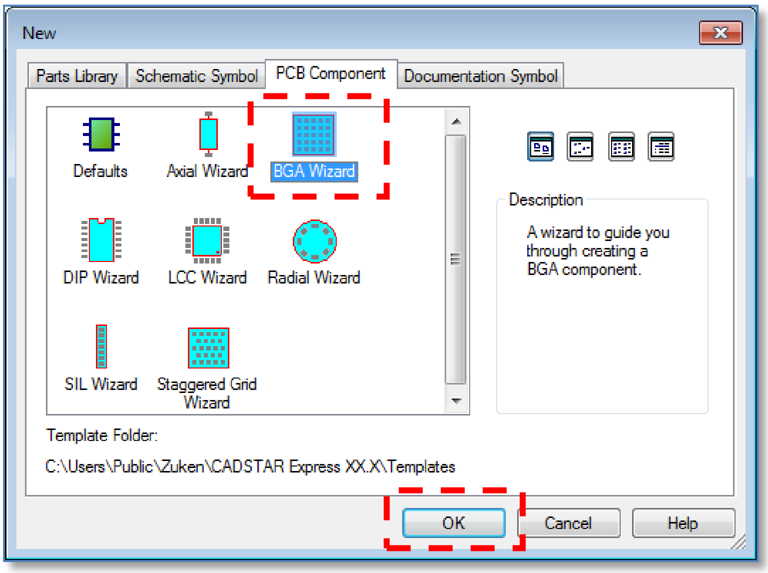

The Library Editor functions as its own CADSTAR Application. It uses a multi-document interface to edit PCB components, Schematic symbols, Documentaiton symbols and Parts.



We will start with a 64 pad ball BGA using the BGA Creation Wizard.

1. From the [**Home**] tab click the **New** button. Then select the [PCB Component] tab and choose the BGA Wizard in the box.

   Click the **[OK]** button



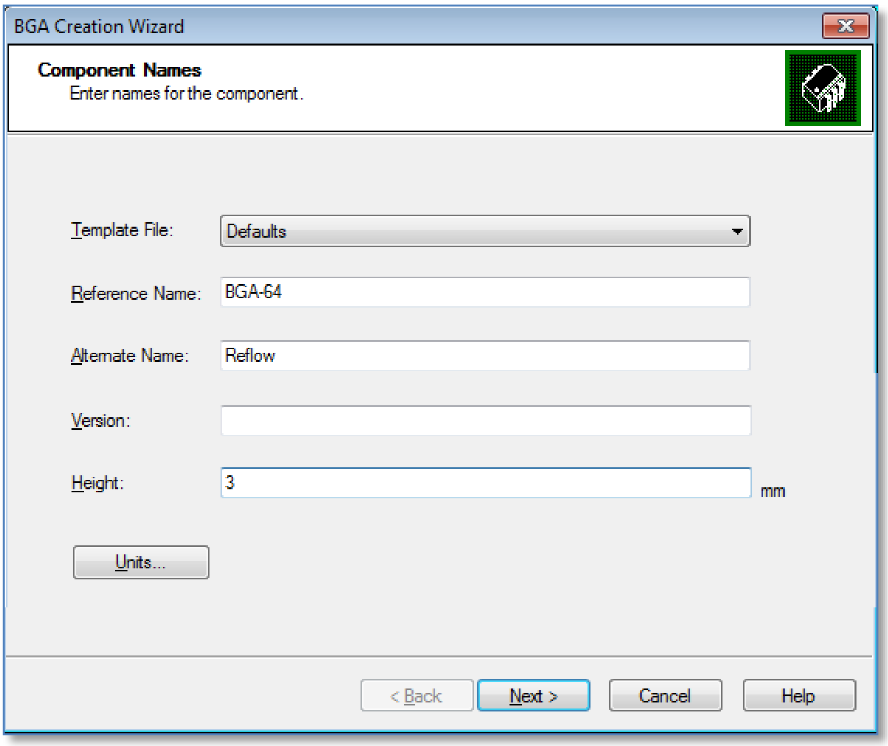

2. Enter a {Component} Reference Name of **BGA-64**. (do not enter BGA64 as demonstrated in the above video link)  Fill in an Alternate Name I.e. **Reflow.**

   Change the **Units** from Thousandths of an Inch to Millimeters.

   This is handy when you have component specifications that are documented in mm or Thou.

   Fill in the component Height if you want to run a Design Rule Check on the height clearances, which can be checked against placement areas as defined in the Design Editor, or you can run a collision check in BoardModeler Lite.

   As this is a new component, the version will be 1.




   If *Automatic Version Increment* in **[File]** tab→ **Options [System]** is enabled, with every future change of the component the version increments automatically. This can easily be checked if the component in the design is the latest version as in the library.

   Select **[Next >]**

3. Enter the assignments to be used for pads and outlines.

**Pads:** Choose for the Pads the pre-defined pad Code *bga64r.*

**Side:** When you are creating an SMD component seen from Top View you must select the *Min* side to place the SMD pads on component side.

**Origin:** The component *Origin* should be placed for SMD components *at centre.*

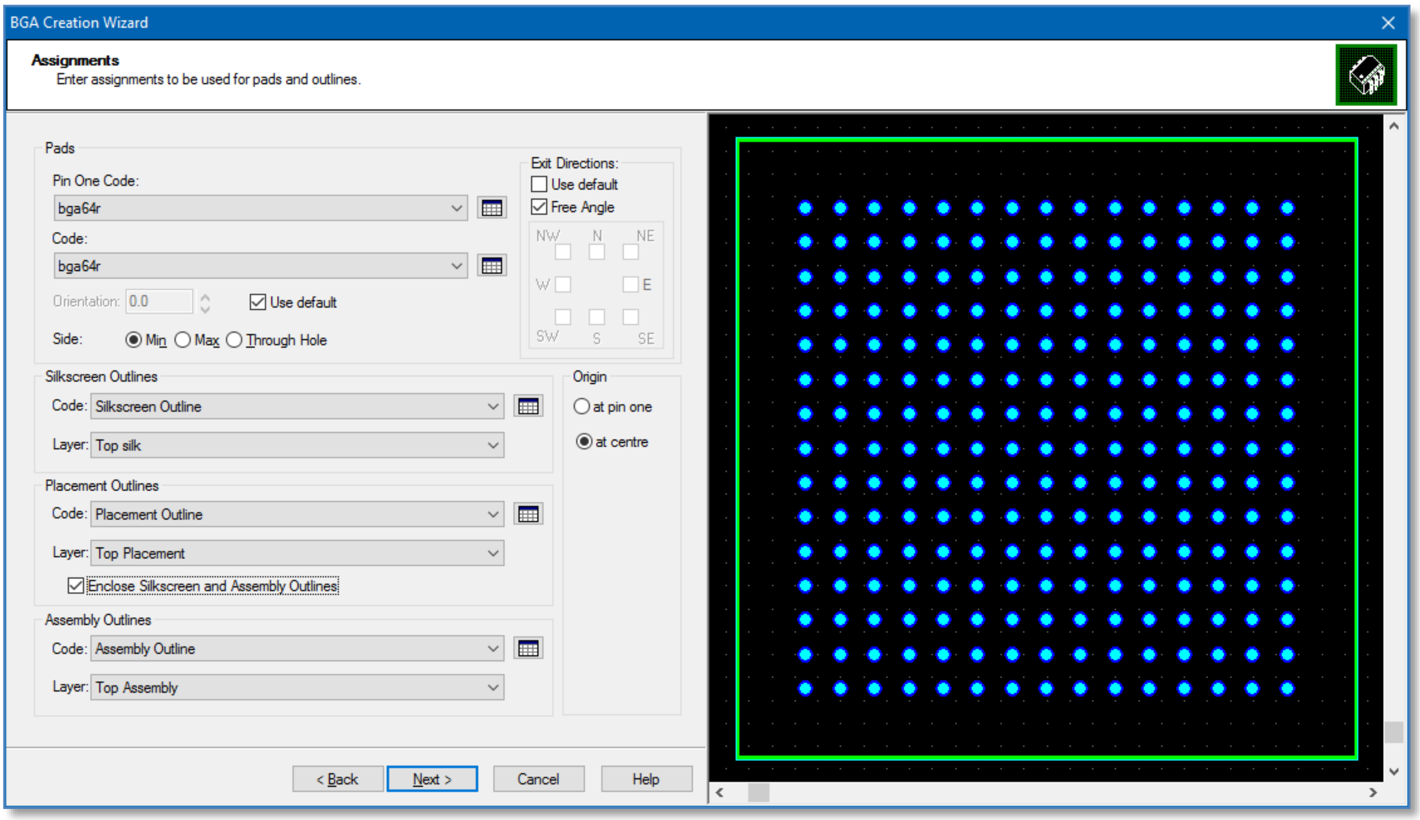
**Silkscreen Outlines:** The Code specifies the thickness of the line you are drawing. For Layer you should select Top silk.

**Placement Outlines**: The Code specifies the thickness of the line you are drawing. For Layer you should select Top Placement.

Check the option for Enclose Silkscreen and Assembly outlines as shown below.

**Assembly Outlines:** The Code specifies the thickness of the line you are drawing. For Layer you should select Top Assembly.

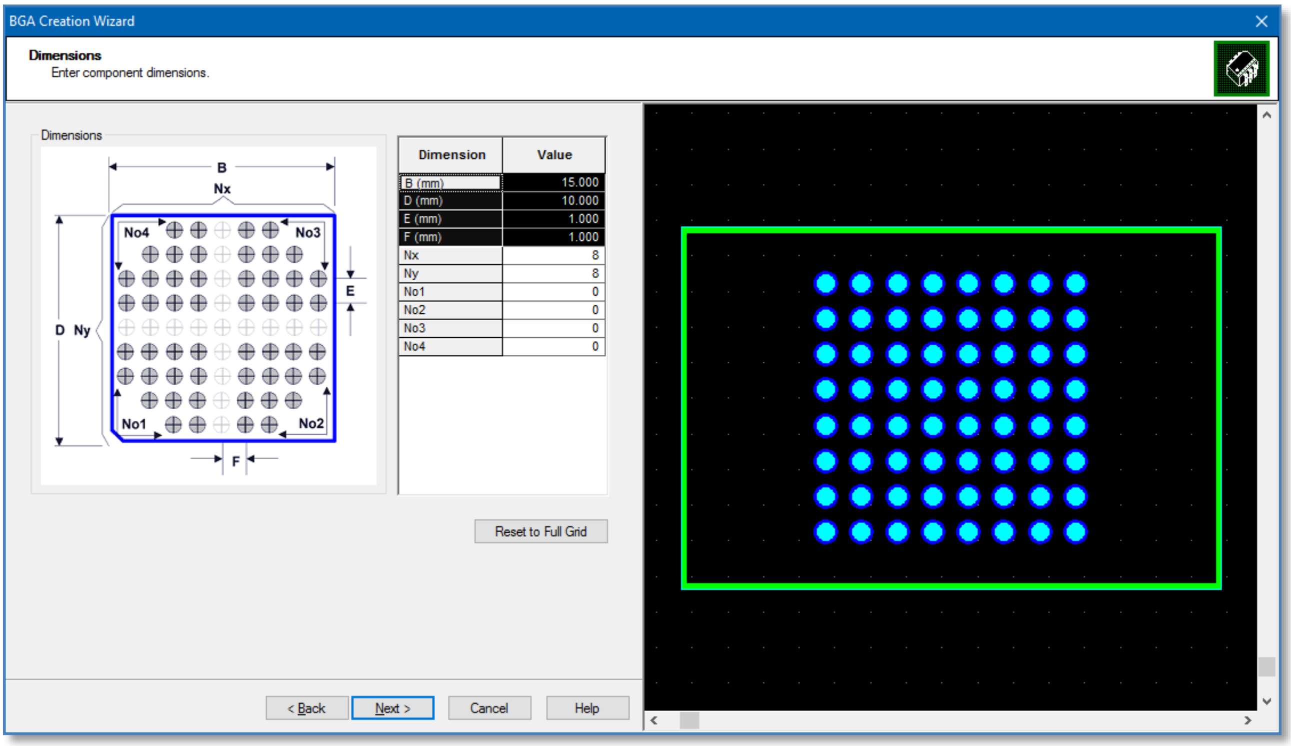
**Note:** These layers are referenced in the PCB Layer settings as layer sub types and are used by other features.




Select **[Next >]**

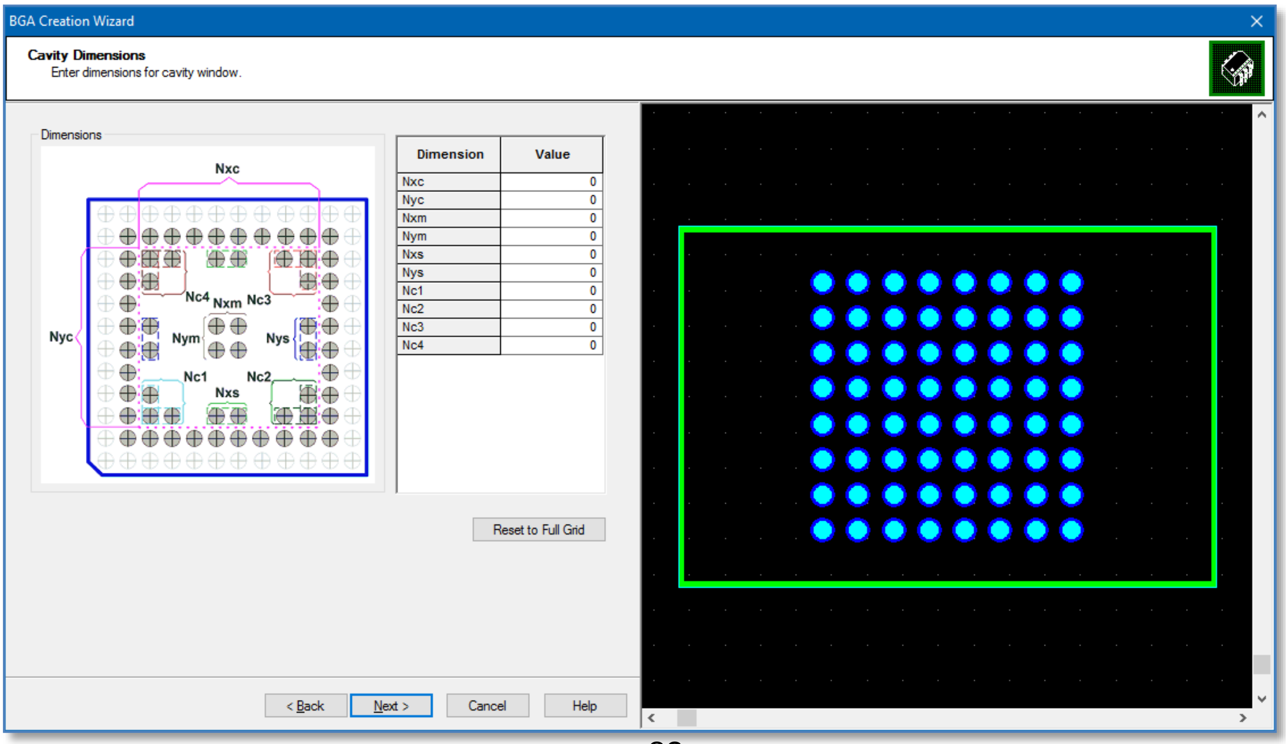
4. Enter the component dimensions:

   Set B to: 15 mm
   Set D to: 10 mm
   Set E to: 1 mm
   Set F to: 1 mm
   Set Nx to: 8
   Set Ny to: 8

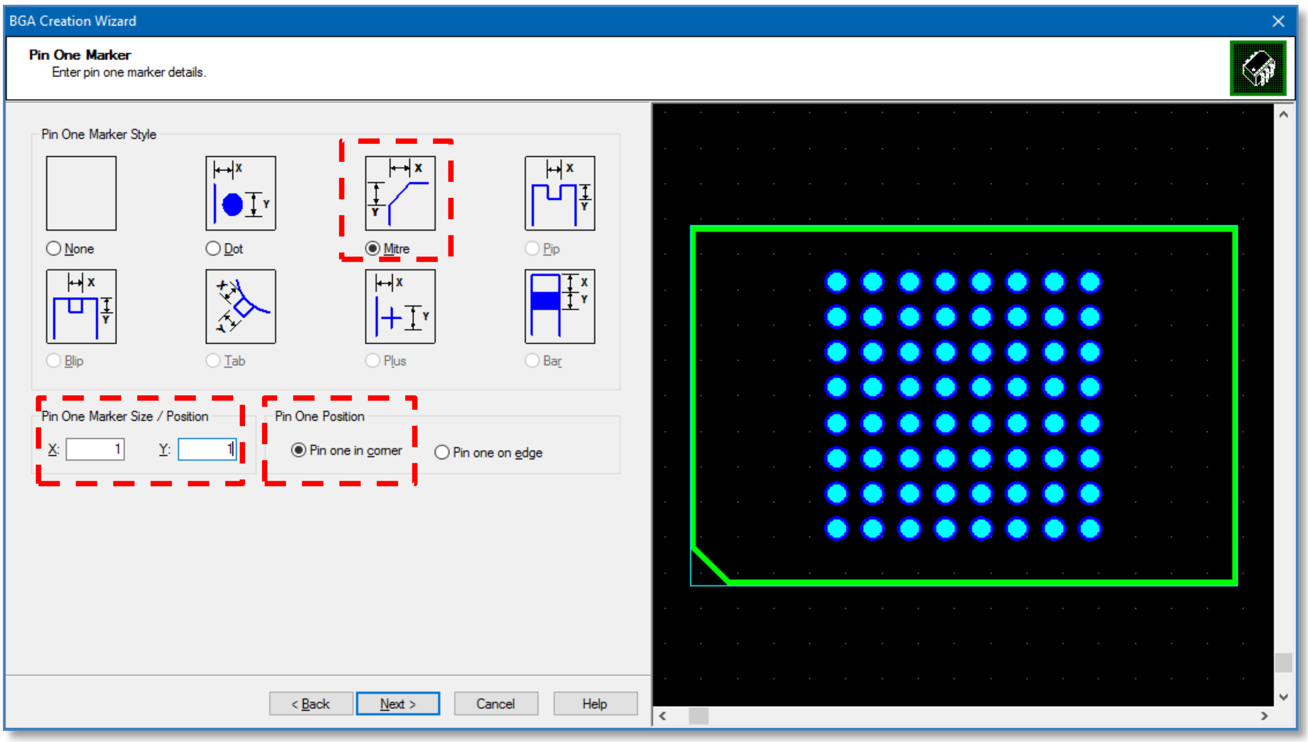



Select **[Next >]**

The next dialog is for designing the cavity dimensions where BGA pads are subtracted to match the physical component package. For this task we will skip this option. Come back later and experiment with this option. Select: **[Next >]**

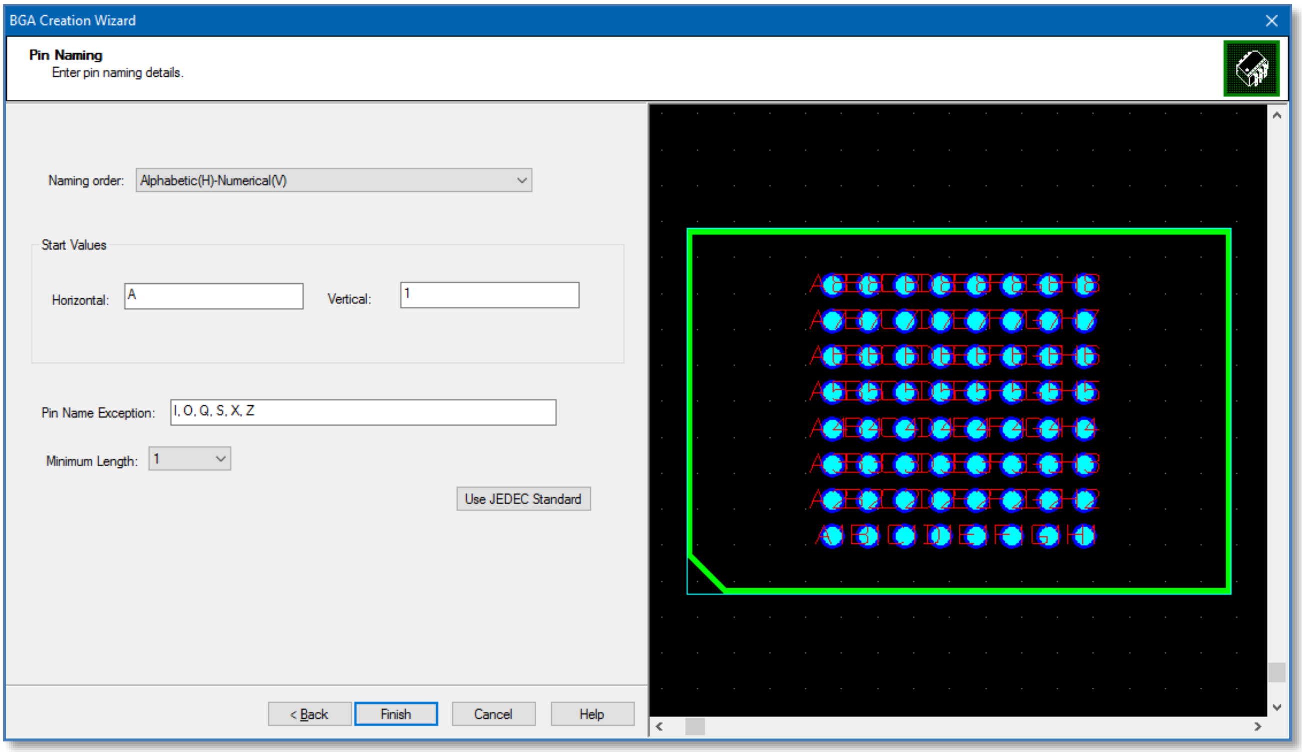


5. Decide how the "Pin 1" marker location will appear on the component (this will ensure the correct mounting of the device). Set the options as shown in the image.

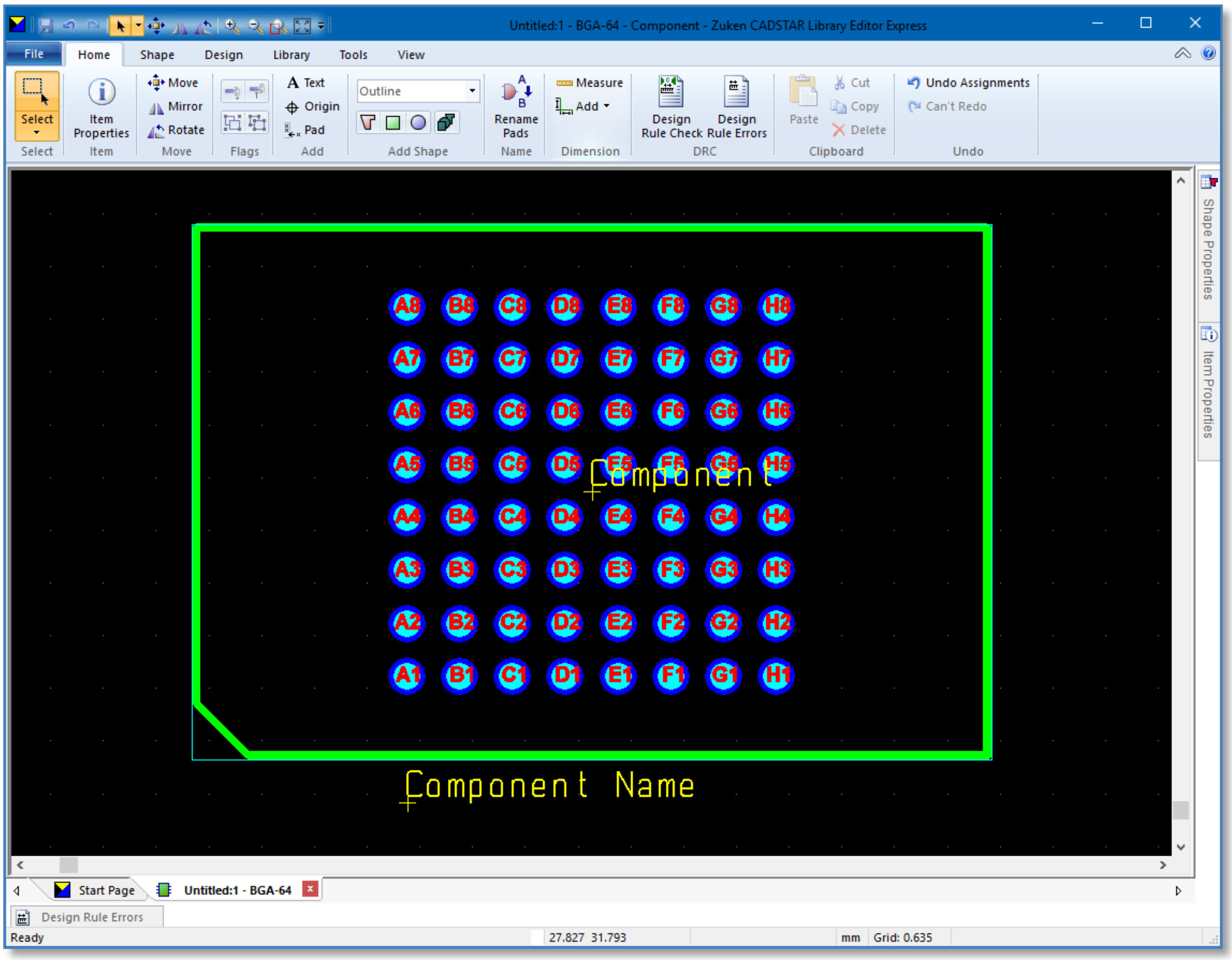



Select: **[Next >]**

6. Last, we will assign the pin names to the BGA pads.



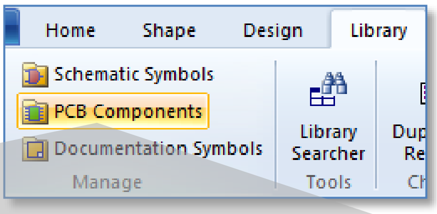

At this stage, you can **[Finish]** the wizard and the **BGA-64(Reflow)** will be created and displayed in the component editor where you can still modify the PCB component manually if needed.

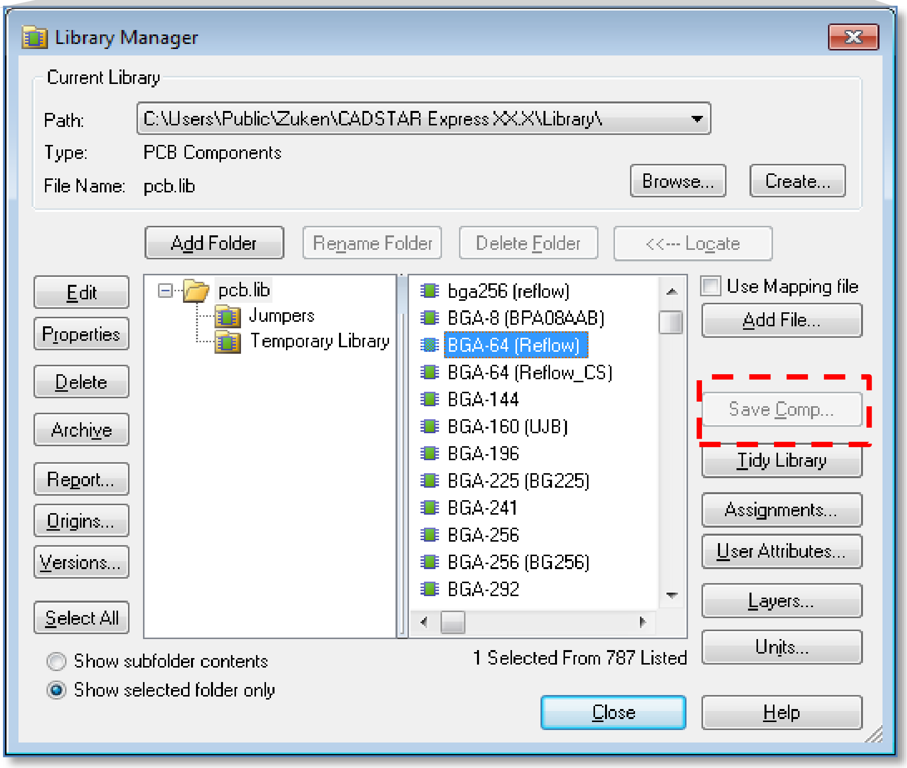



7. When done, save the component.

Click on the [**Library**] tab→ **PCB Components** – [**Save Comp**].

If the component already exists in the library you can decide to over-write it if you wish.



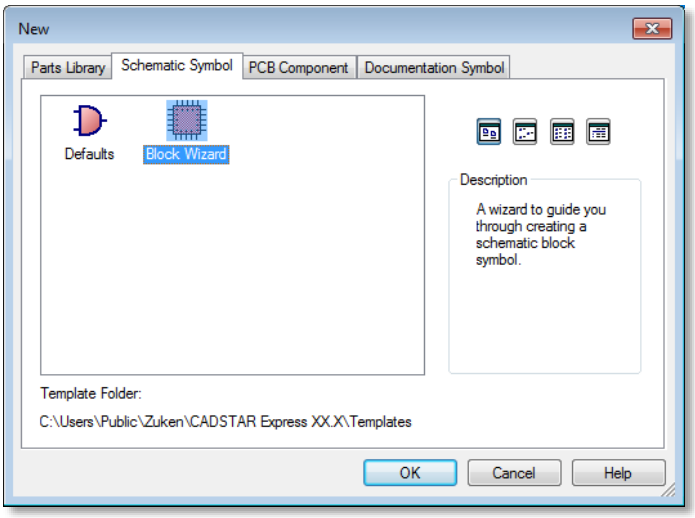
## Step 2 - Schematic Symbol / Block Wizard

We shall start with going through the Schematic Block Creation Wizard. The symbol to create is a StrataFlash® Embedded Memory device.  This device is built up with 2 schematic symbols therefore we will use the multiple gate functionality.

1. Select **[File]**tab→**New**→**[Schematic Symbol]** and choose the **Block Wizard** in the box.

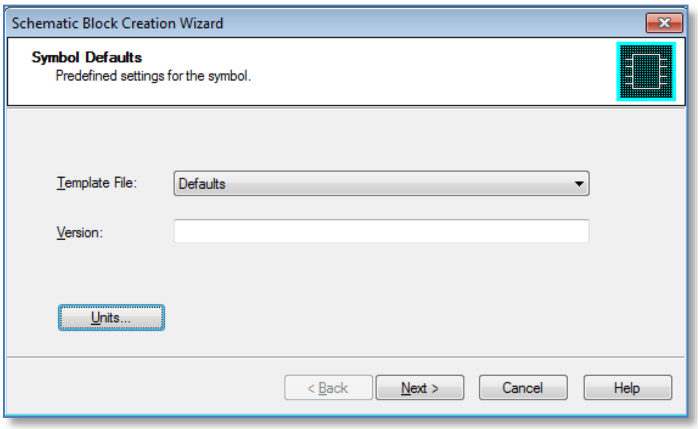
   We will start by creating the power symbol and logic symbol concurrently.

   Click **[OK]**




2. You can choose a different template file. In addition you can also fill in the version number (1 as this is a new symbol). [Units] can also be changed to suit your specification. For this step set them to Thou.

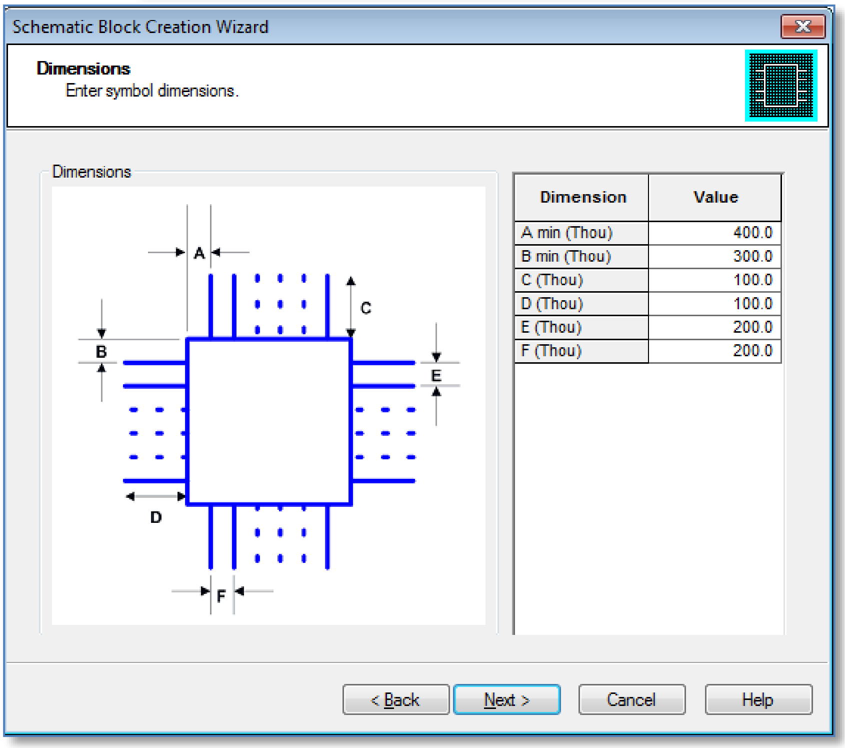
   Select **[Next >]**




3. The second step is to enter the symbol dimensions as shown.

   **Tip:** The size of the text font used in the data can be made more legible by holding down the <ctrl> button and scrolling the mouse wheel.

   Select **[Next >]**



4. The next step is to add a gate, number of pins, define the pin locations and to fill in the Reference Name. In addition you can also fill in the Alternate Name.

   Select *Gates* – **[Add]** one gate.

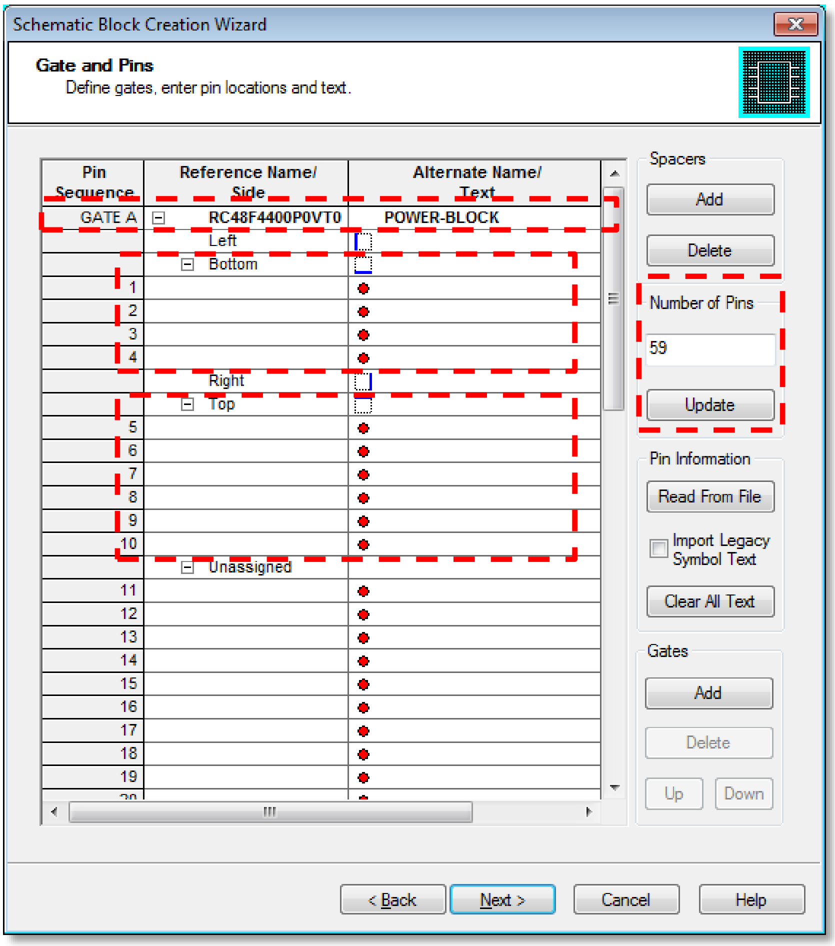
   For GATE A, enter the *Reference Name* as **RC48F4400P0VT00-P**
   and *Alternate Name* **POWER-BLOCK**

   For GATE B you can fill in the *Reference Name* **RC48F4400P0VT00**

   Set the *Number of Pins* to **59** and select **[Update]**.

   Select the *Pin Sequence* numbers 1 to 4 by using the CTRL/SHIFT key and drag and drop the *Pin Sequence* column to *Bottom* of GATE A, as shown to the right.

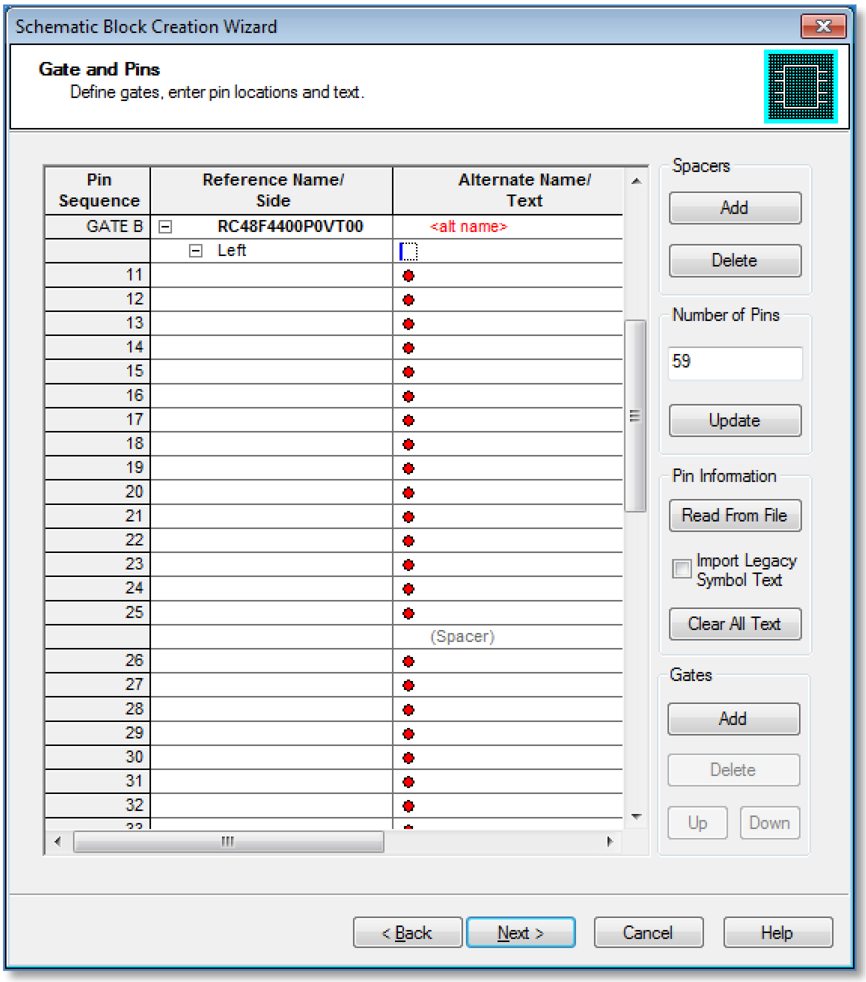
   Select *Pin Sequence* numbers 5 to 10 by using the CTRL/SHIFT key and drag and drop the *Pin Sequence* column to *Top* of GATE A as shown to the right.




**Tip:** Once you have selected a group of pins, you may also try clicking the <**R.M.B.**> to access an assist dialog.

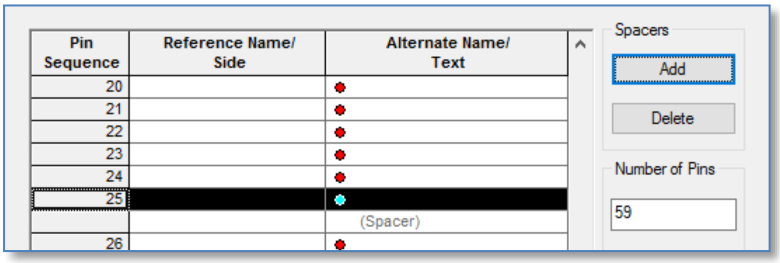
Select the *Pin Sequence* numbers 11 to 43 by using the CTRL/SHIFT key and drag and drop the *Pin Sequence* column to *left for GATE B* as shown.

Select *Pin Sequence* numbers 44 to 59 by using the CTRL/SHIFT key and drag and drop the *Pin Sequence* column to *right of GATE B.*




The *spacers* are equal to the pin spacing assigned previously.

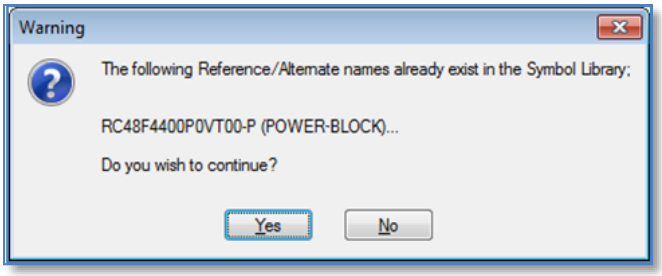
Add a *spacer* in between pins 25 and 26 by clicking on the pin 25 row and then clicking the [ADD] button.




Select **[Next >]**

As a courtesy check once you get to this point, you may get a warning if the Symbol Reference/Alternate name exists in the Symbol Library.

This gives you the opportunity to take action. In this case select [Yes]



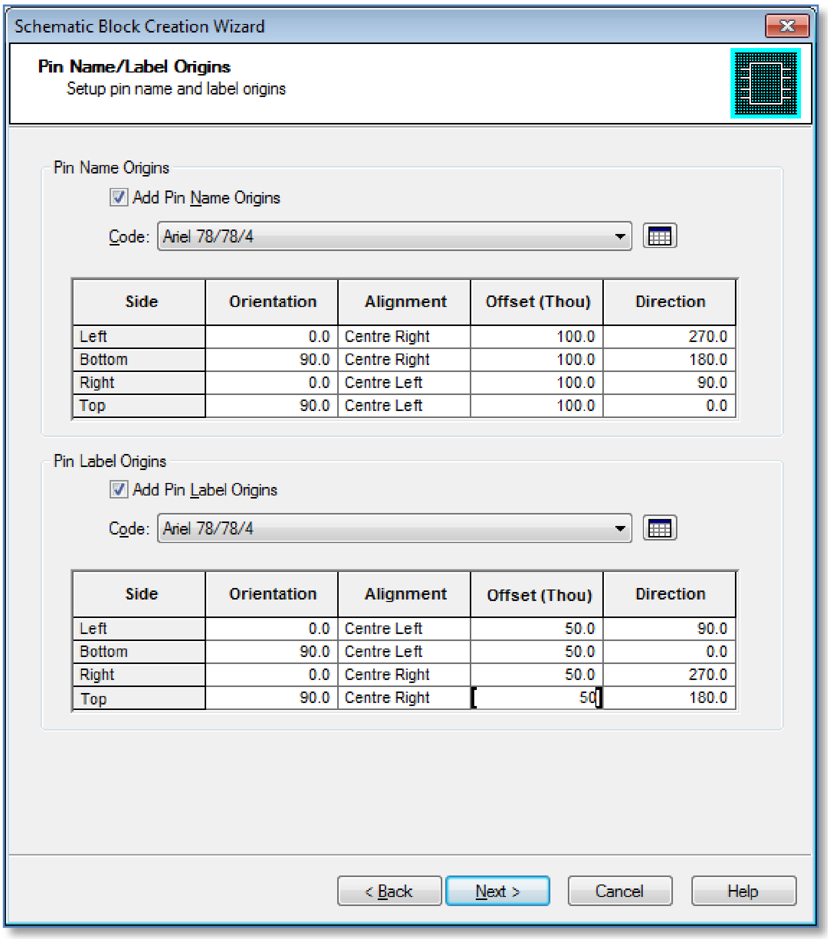
5. The next step is to enter the Pin Name/Number and Pin Label Origins.

   The position of the *Pin Name / Numbers* and *Pin Labels* are related to the final pin position.

   **Note:** By default the Wizard will place Pin Name/Number and Pin Label Origins intuitively, with Pin Names outside the block, and Pin Labels inside.

   Ensure the settings are the same as the example. →

   Select **[Next >]**




6. The last step is to enter assignments to be used for terminals and outlines.

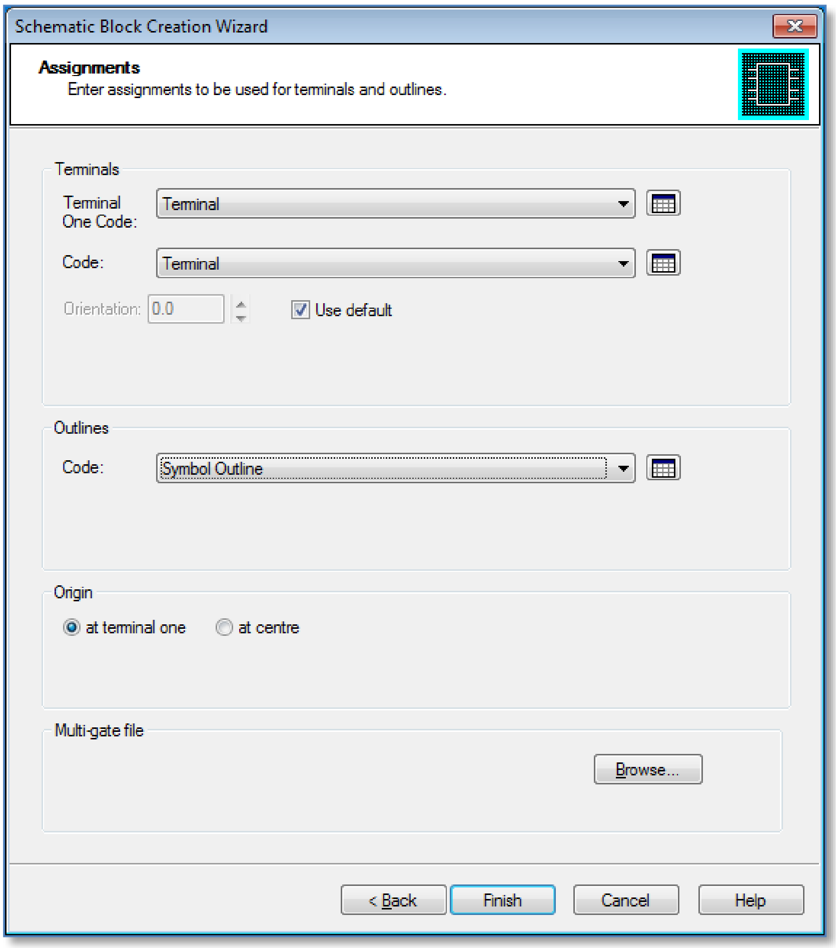
   **Terminals:** Set the Terminal Codes to *Terminal.*

   **Outlines:** The *Outline Code* specifies the thickness of the line drawing. You should select *Symbol Outline.*

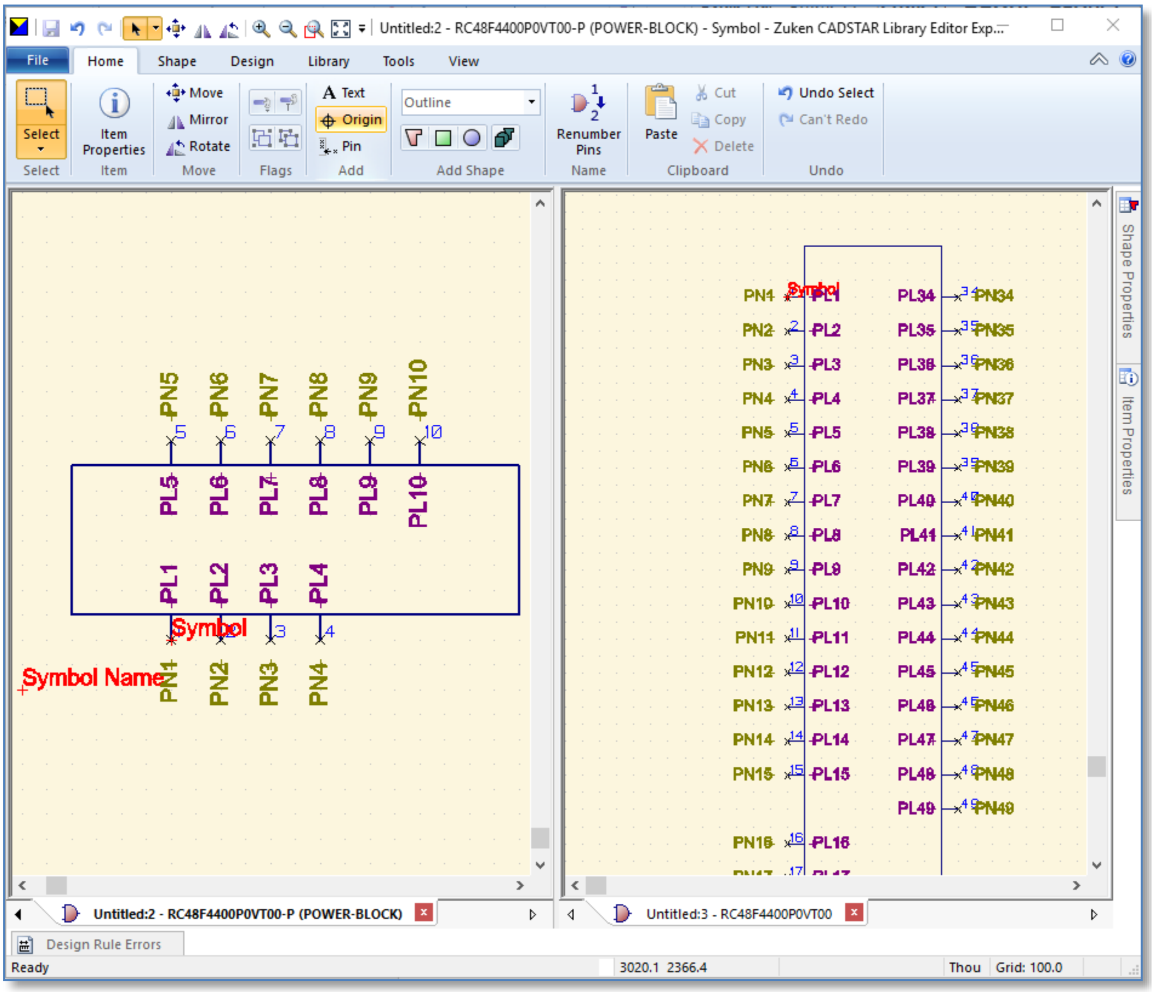
   **Origin:** The symbol *Origin* should be placed *at terminal one.*

   At this stage, you can **[Finish]**

   Select **[No]** if you are asked to set the multiple gate file, this is only needed when reading an Aldec FPGA pin list file (CSV).



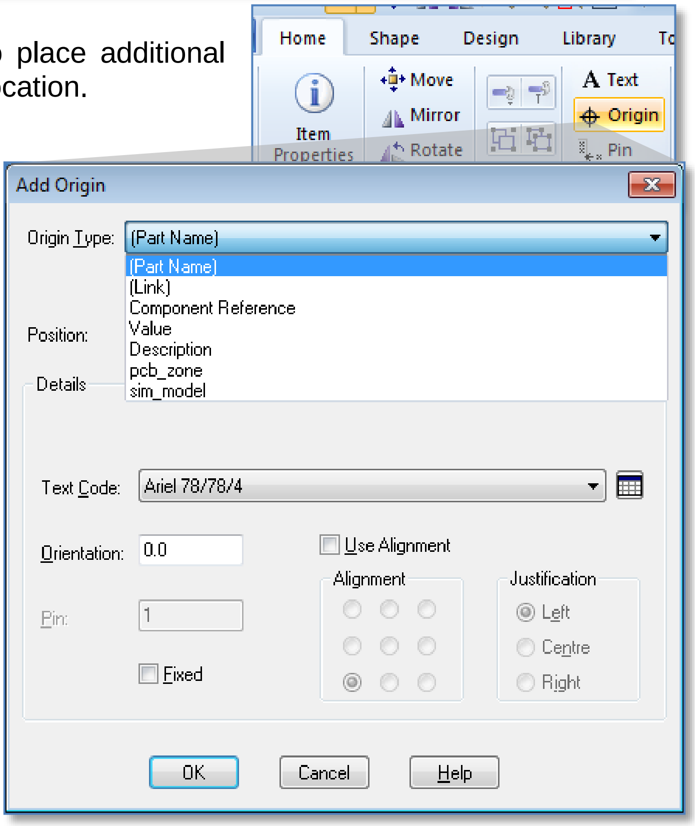
The symbols will be created and appear in separate windows. You may choose to modify them to suit your requirements.



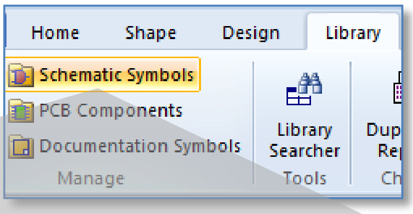

7. Select the Add Origin tool bar icon to place additional origins such as the default Part name location.

Simply browse the *Origin type* list and select the origin name you wish to place.

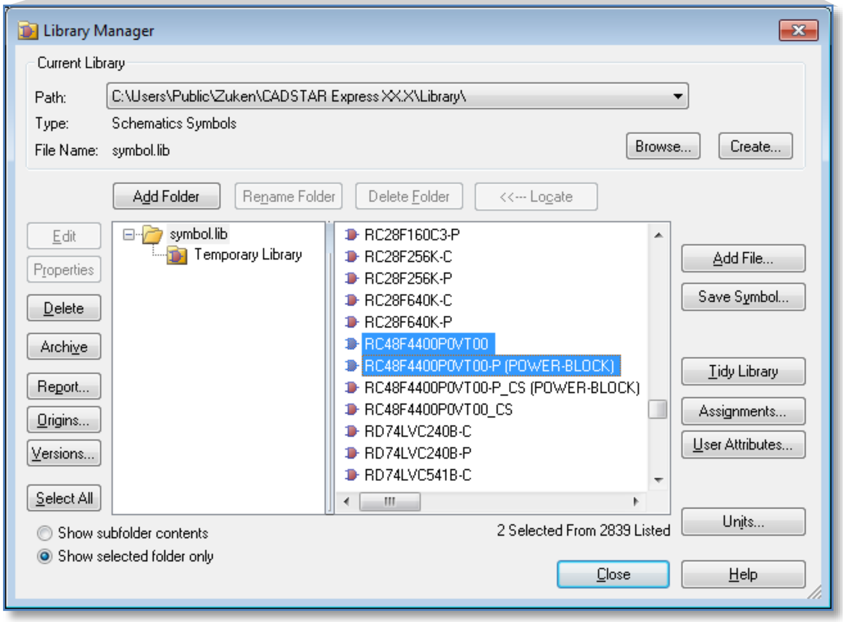
Try adding the **(Part Name), (Link)** and **Description** to both symbols.



8. You can still modify the schematic symbols manually if needed. When done, save them by clicking on the **[Library] →Schematic Symbols [Save Symbol]** button.

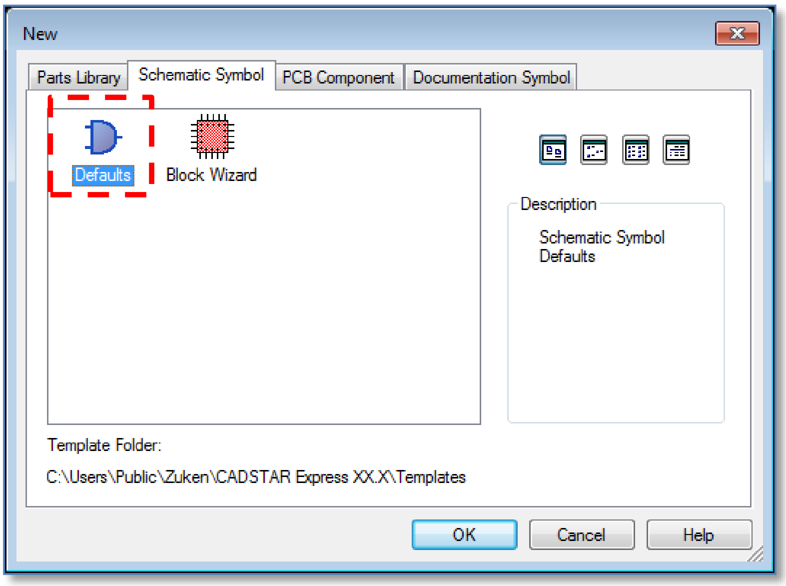



If the symbol already exists in the library you can decide to overwrite it if you wish.




You can now go through the Schematic Block Creation Wizard again and create another device if you wish.

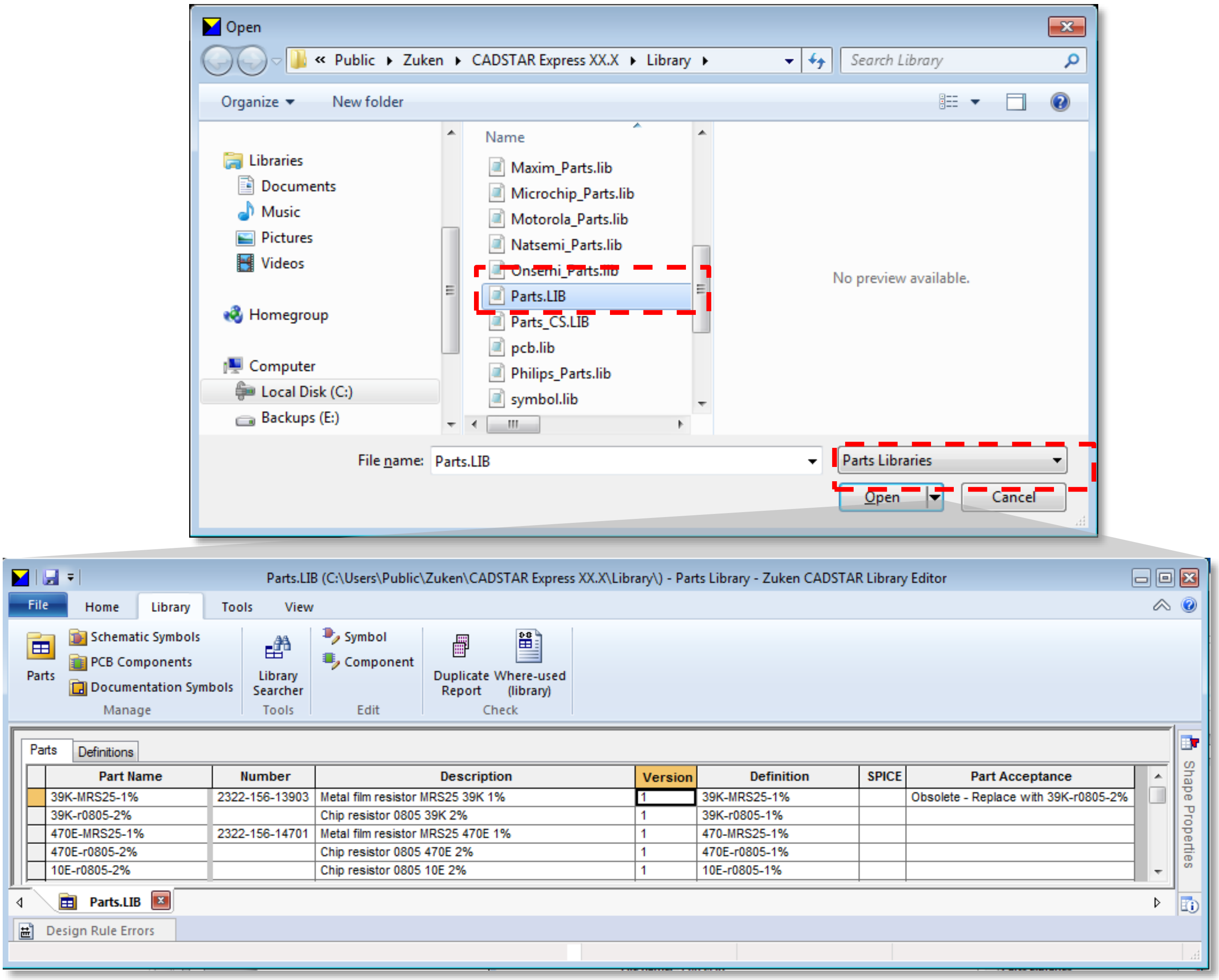
Another option is to select the Defaults option which will open an empty symbol window where you can create symbols from scratch.



## Step 3 - Parts Library Editor

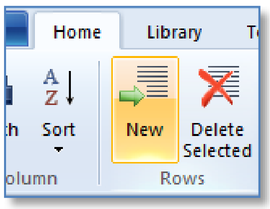
Now that you have created the PCB component and the two schematic symbols you can generate the Part definition that will link the schematic symbols and PCB component together.

1. From within the Library Editor click on **[File]** tab→**Open.** Click [**Browse the Library directory**] and open “Parts.lib”. **Tip:** Change the file type to Parts Libraries as shown below.

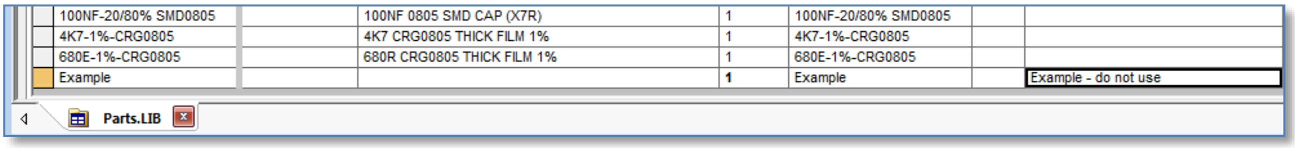



**Tip:** The size of the text font used in the tables can be made more legible by holding down the <ctrl> button and scrolling the mouse wheel to zoom in and out.

2. From the **[Home]** tab click the **New** icon for ***Add New Row*** →



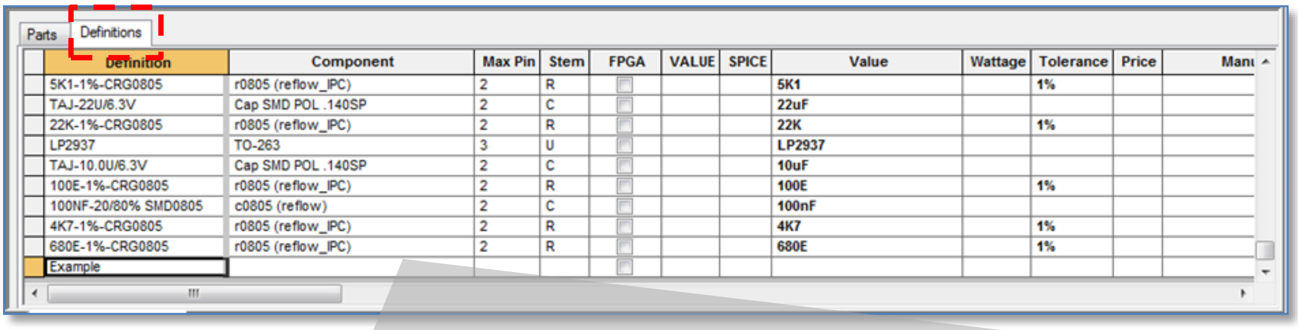
When creating Part Definitions,you must fill in the ***Part Name*** and ***Definition*** column fields (in both fields type: "**Example"** as shown below.) In addition you can fill in the Description if you want to run a more detailed Parts List of the used components in your design.



| | | | | | | |
|---|---|---|---|---|---|---|
| 100NF-20/80% SMD0805 | | 100NF 0805 SMD CAP (X7R) | 1 | 100NF-20/80% SMD0805 | | |
| 4K7-1%-CRG0805 | | 4K7 CRG0805 THICK FILM 1% | 1 | 4K7-1%-CRG0805 | | |
| 680E-1%-CRG0805 | | 680R CRG0805 THICK FILM 1% | 1 | 680E-1%-CRG0805 | | |
| Example | | | 1 | Example | | Example - do not use |



3. Change the spreadsheet from [**Parts**] tab to [**Definitions**] tab by clicking on the Definitions tab.

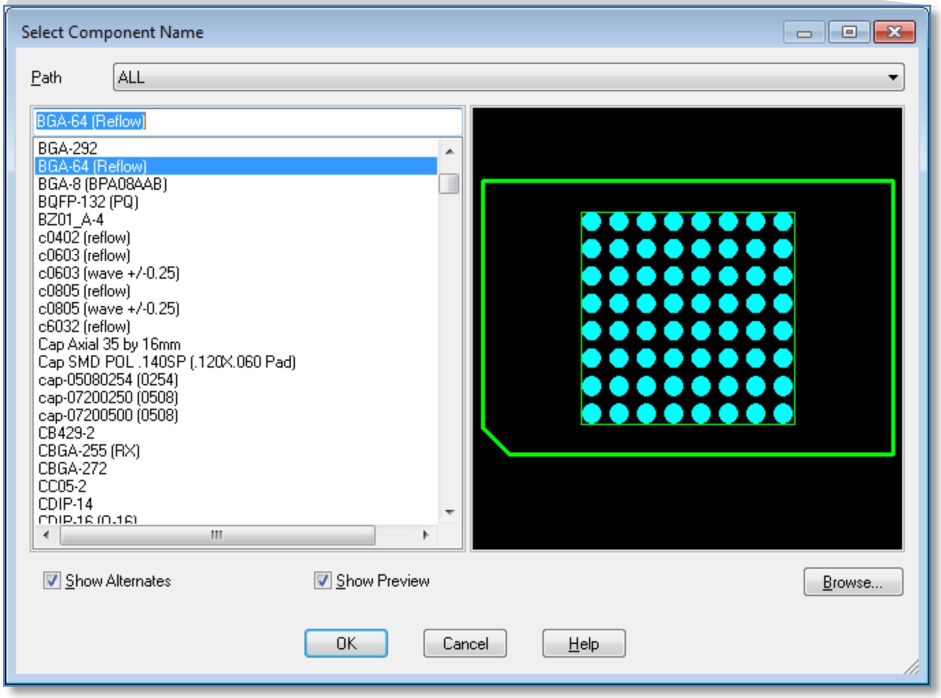




| Definition | Component | Max Pin | Stem | FPGA | VALUE | SPICE | Value | Wattage | Tolerance | Price | Manu |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5K1-1%-CRG0805 | r0805 (reflow_IPC) | 2 | R | | | | 5K1 | | 1% | | |
| TAJ-22U/6.3V | Cap SMD POL .140SP | 2 | C | | | | 22uF | | | | |
| 22K-1%-CRG0805 | r0805 (reflow_IPC) | 2 | R | | | | 22K | | 1% | | |
| LP2937 | TO-263 | 3 | U | | | | LP2937 | | | | |
| TAJ-10.0U/6.3V | Cap SMD POL .140SP | 2 | C | | | | 10uF | | | | |
| 100E-1%-CRG0805 | r0805 (reflow_IPC) | 2 | R | | | | 100E | | 1% | | |
| 100NF-20/80% SMD0805 | c0805 (reflow) | 2 | C | | | | 100nF | | | | |
| 4K7-1%-CRG0805 | r0805 (reflow_IPC) | 2 | R | | | | 4K7 | | 1% | | |
| 680E-1%-CRG0805 | r0805 (reflow_IPC) | 2 | R | | | | 680E | | 1% | | |
| Example | | | | | | | | | | | |

Here, you can;

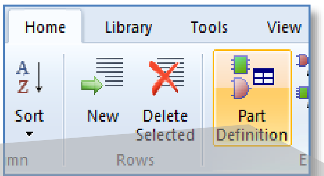
- Choose a component reference shape I.e. **BGA-64 (Reflow)** by double clicking in the cell to open the browser
- Enter a default ref-des prefix or *Stem **"U"***
- Enter attribute information





The basic idea is that multiple Part names can reference the same Definition. However depending on your future Library creation plans, you may choose to reference only one part name per definition.

4. Select the new part definition row for “Example” and click on the **[Home]** tab and the **Part Definition** button to edit. (or use the right mouse button menu).

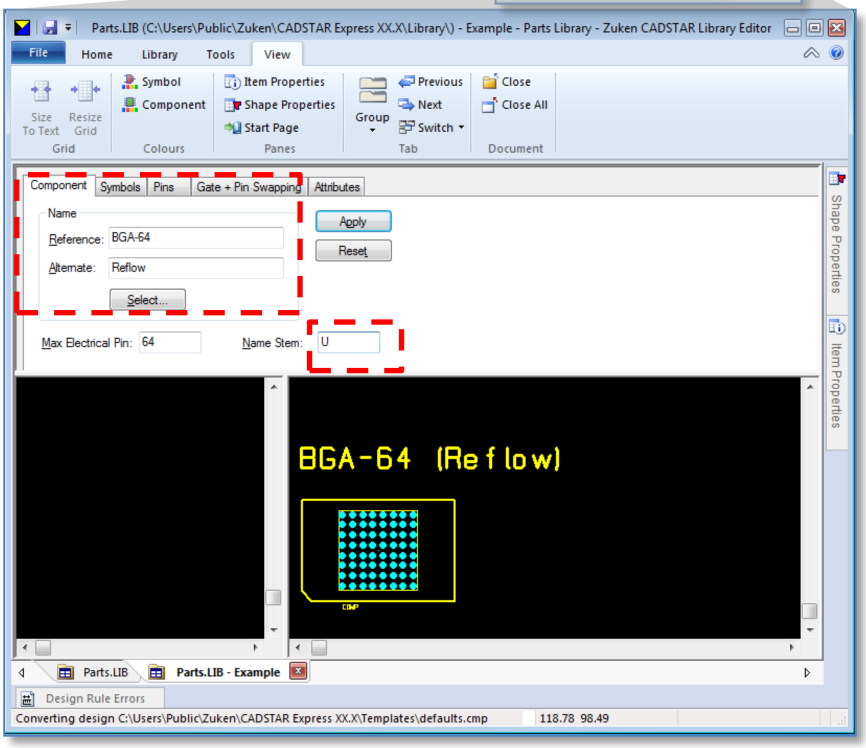


5. From the [**Component**] tab, click the [**Select**] button and choose the PCB Component **BGA-64(Reflow)** that you created by using the BGA Wizard in the previous exercise.

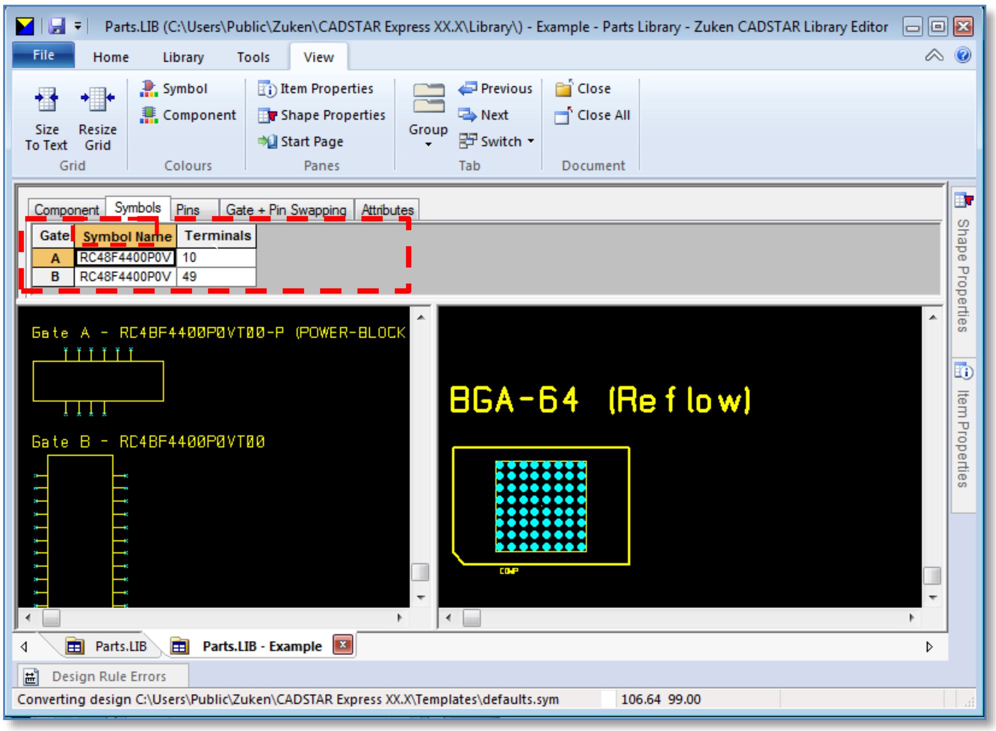
   Set the **Name Stem** to: ***U***

   This is the prefix for the Reference Designator that will be used when the part is added to a Design.

   **Note:** both the Component name and Name stem could have been entered on the Definitions tab in step 3.



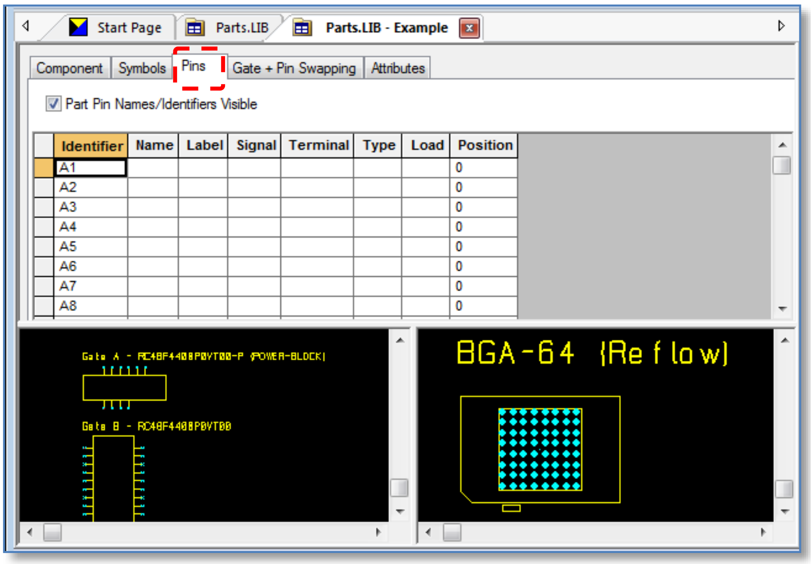
6. Select the [**Symbols**] tab and click the **New** button shown on the **[Home]** tab to add a second row for gate B.



7. Double-click in the Symbol Name field or use the right mouse button menu [Select Symbol..] and select, for Gate A, the symbol RC48F4400P0VT00-P(POWER-BLOCK) you created by using the Schematic Block Creation Wizard in the previous exercise. For Gate B select the Symbol RC48F4400P0VT00.

   **Tip:** Start typing the symbol name and the searcher will take you quickly to the symbol name

8. Select the [**Pins**] tab.



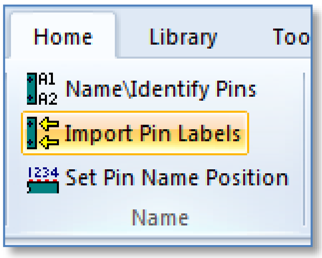

   From here, the physical pins of the Component reference shape ***BGA-64(Reflow)*** will be mapped to the pins of the two schematic gates.

   Additional pin information can also be entered.

   Note that the Alpha-numeric pin names of the component are listed in the *Pin* column. These names will be displayed on the schematic symbol pin locations once mapped.

   Also note that when using Components reference shapes that contain Alpha-numeric pin names it is not necessary to enter pin names in the table.

9. Click on the **Import Pin Labels** button located on the **[Home]** tab.



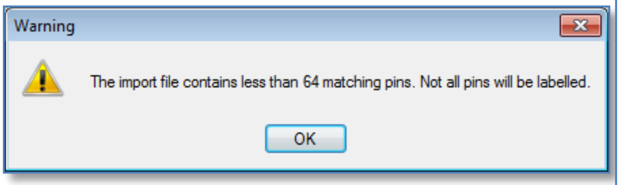

   Rather than importing a pin label for each pin name a *pinname* list file has been provided in *C:\....\Zuken\CADSTAR Express XX.X\Self Teach.*

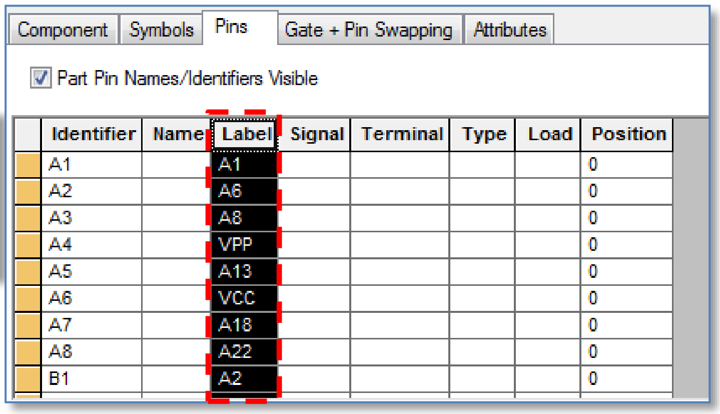
   Select the file name: ***pinlist.pin*** click **[Open]**

   **Tip:** A pin list can be often down-loaded from the component manufacturer's website or you can extract it from the component manufacturer datasheet in spreadsheet software (for example MS Excel).

CHIP ← *{Header}*
A1: pinname (colon)
A6: .
A8: .
VPP: .
A13: .
VCC: .
A18: .
A22: .
A2: . <cr><lf>

If the Pin list has less pins than what is in the [**Pins**] tab you will get the warning shown below.

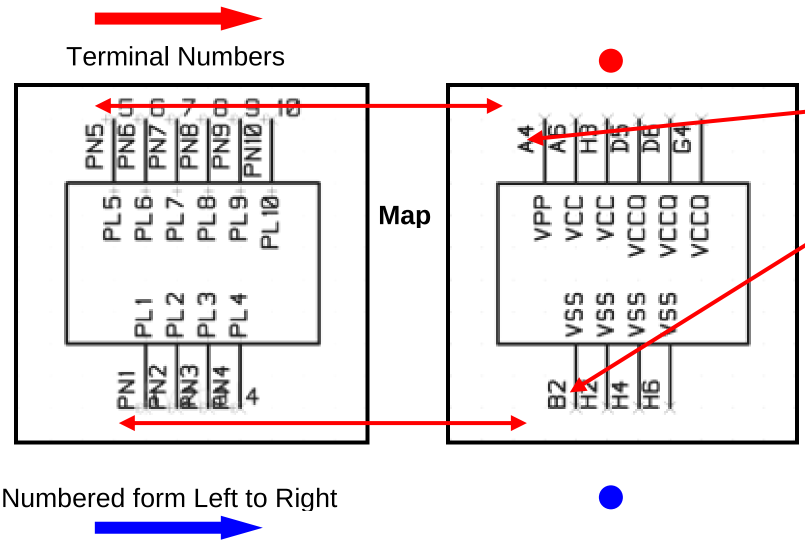




Component | Symbols | Pins | Gate + Pin Swapping | Attributes

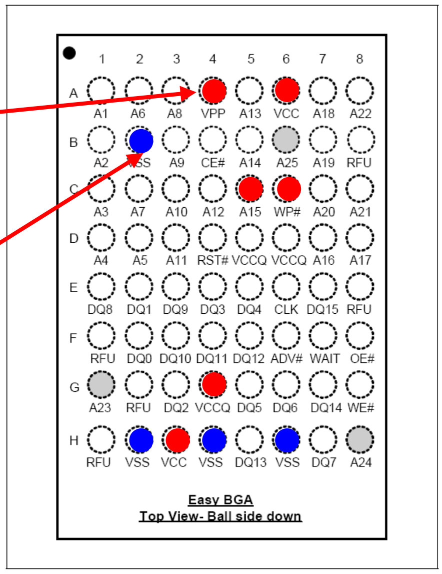
Part Pin Names/Identifiers Visible

| Identifier | Name | Label | Signal | Terminal | Type | Load | Position |
|---|---|---|---|---|---|---|---|
| A1 | | A1 | | | | | 0 |
| A2 | | A6 | | | | | 0 |
| A3 | | A8 | | | | | 0 |
| A4 | | VPP | | | | | 0 |
| A5 | | A13 | | | | | 0 |
| A6 | | VCC | | | | | 0 |
| A7 | | A18 | | | | | 0 |
| A8 | | A22 | | | | | 0 |
| B1 | | A2 | | | | | 0 |

When you used the Schematic Block Wizard for the creation of the first symbol *(RC48F4400P0VT00-P)* a total of 10 terminals were placed on the bottom and top side of the symbol and if you remember, they are always numbered from left to right. Usually the VSS is placed at the bottom of the power symbol and the VCC at the top.

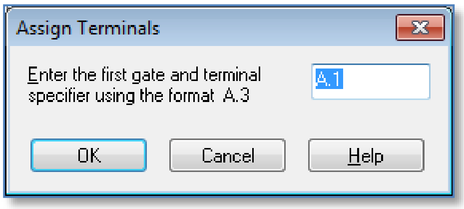



**64-Ball Easy BGA Ballout (64/128/256/512-Mbit)**

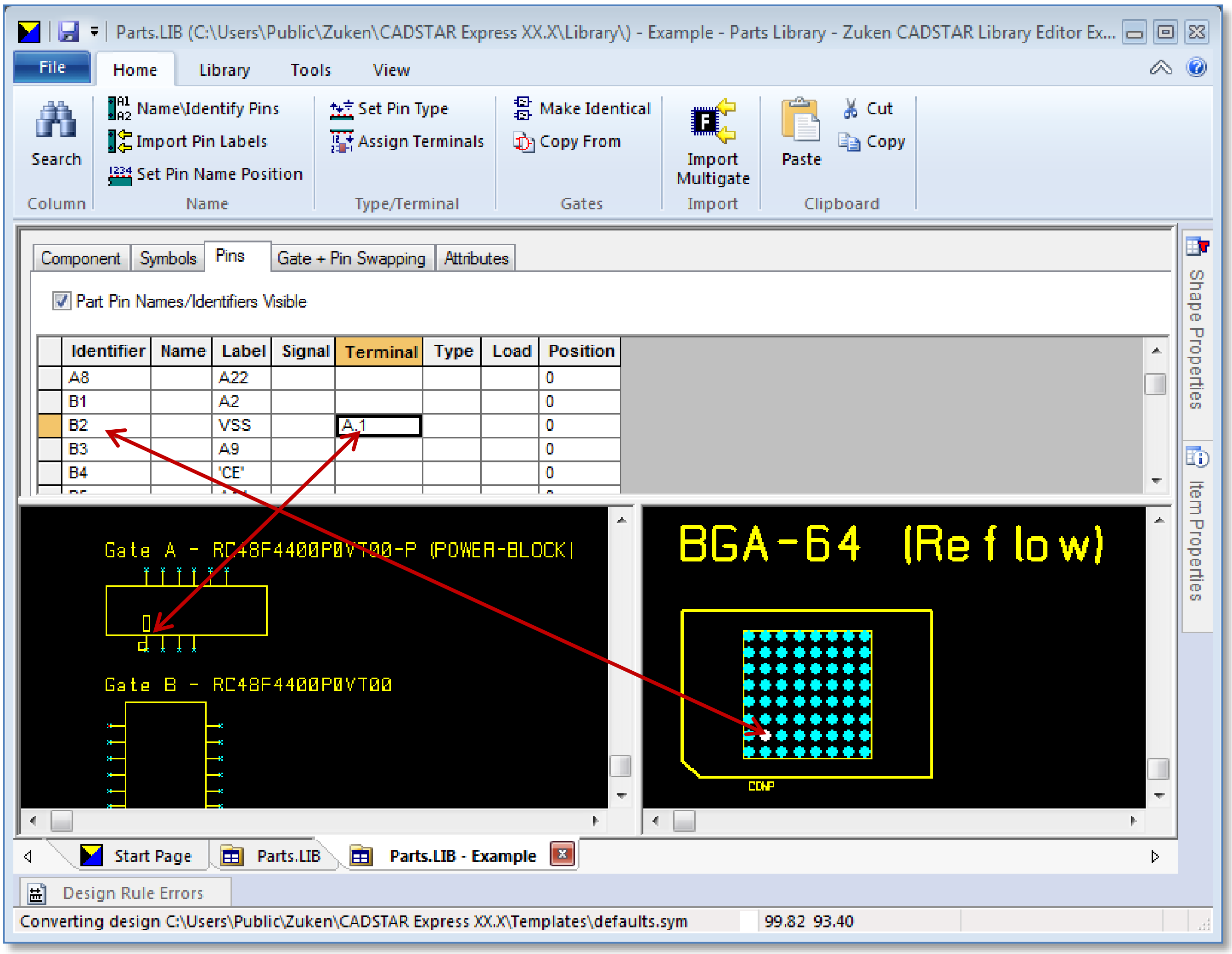



10. The next step is to map the symbol terminals with the accompanying Pin Numbers/Names (and Labels).

    In other words you will start with the pin *B2* (Label *VSS)* assigning it to Terminal A.1 = {Gate A. symbol terminal 1}



Select the Terminal cell belonging to Pin Name B2 (Label VSS), and select **Assign Terminals** or use the right mouse button menu and select **Assign Terminals** or Just double click in the cell.



Now you can finish the mapping for the power symbol by selecting, in the correct order, the next power pins.

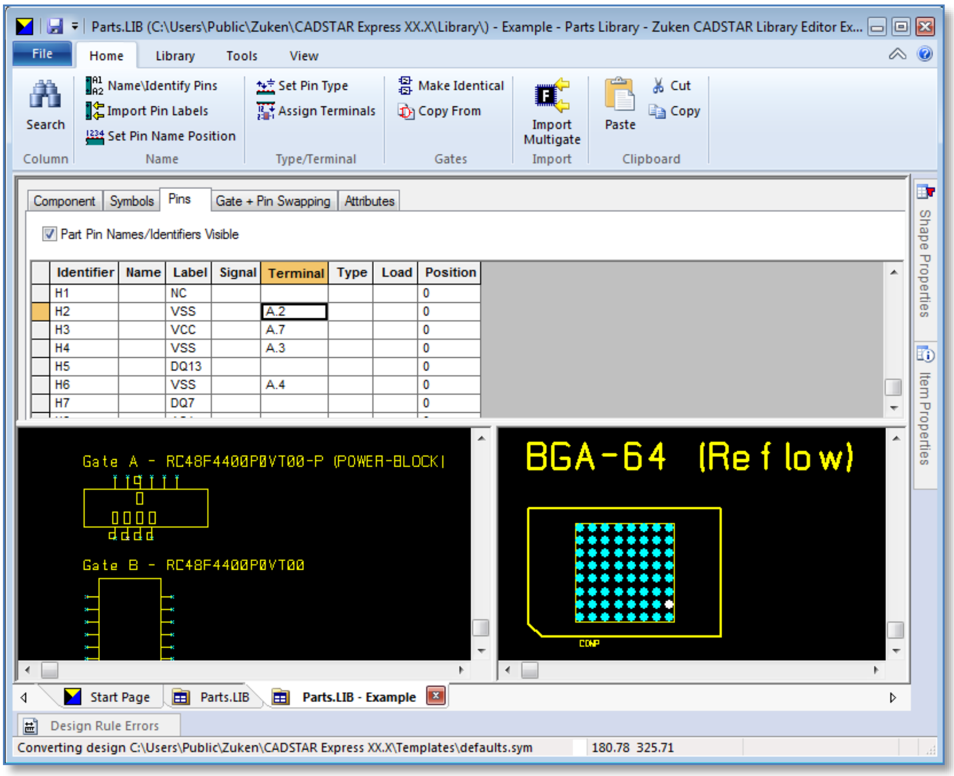
Look for pin *H2* (Label *VSS*) and click in the terminal field. You will notice that automatically A.2 will be assigned.

As you assign the terminals the Pin name labels will appear on the **Gate A** symbol in the preview pane.

**Tip:** If you make a mistake during the allocation of the terminals, don't worry - just press the [**Escape**] key and restart in the correct box with the new start sequence!

Assign the following:

- pin *H4* (*VSS*) to *A.3*
- pin*H6* (*VSS*) to *A.4*
- pin *A4* (*VPP*) to *A.5*
- pin *A6* (*VCC*) to *A.6*
- pin *H3* (*VCC*) to *A.7*
- pin *D5* (*VCCQ*) to *A.8*
- pin *D6* (*VCCQ*) to *A.9*
- pin *G4* (*VCCQ*) to *A.10*




Continue assigning the terminals for Gate B *(RC48F4400P0VT00).* Just click in the terminal field of pin *A1* (Label *A1*) and you will notice that automatically *B.1* ={Gate B .Symbol Terminal 1} will be assigned.

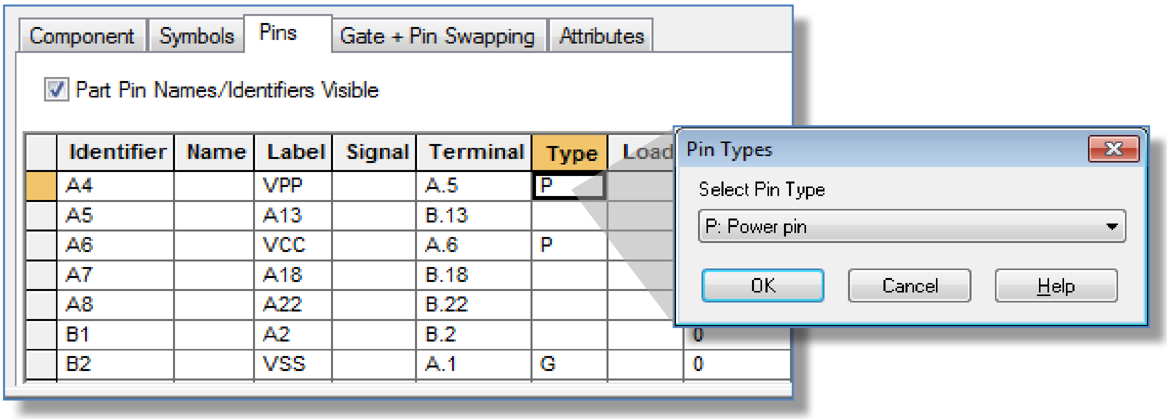
When you used the Schematic Block Wizard for the creation of the second symbol *(RC48F4400P0VT00),* a total of 49 terminals were placed at the left and right side of the symbol and if you remember, they are always numbered from top to bottom.

**Assign following pins for Gate B:**

- pin *A1* ( *A1*) to *B.1*
- pin *B1* ( *A2*) to *B.2*
- pin *C1* ( *A3*) to *B.3*
- pin *D1* ( *A4*) to *B.4*
- pin *D2* ( *A5*) to *B.5*
- pin A2 ( *A6*) to *B.6*
- pin C2 ( *A7*) to *B.7*
- pin A3 ( *A8*) to *B.8*
- pin B3 ( *A9*) to *B.9*
- pin C3 ( *A10*) to *B.10*
- pin D3 ( *A11*) to *B.11*
- pin C4 ( *A12*) to *B.12*
- pin A5 ( *A13*) to *B.13*
- pin B5 ( *A14*) to *B.14*
- pin C5 ( *A15*) to *B.15*
- pin D7 ( *A16*) to *B.16*
- pin D8 ( *A17*) to *B.17*
- pin A7 ( *A18*) to *B.18*
- pin B7 ( *A19*) to *B.19*
- pin C7 ( *A20*) to *B.20*
- pin C8 ( *A21*) to *B.21*
- pin A8 ( *A22*) to *B.22*
- pin G1 ( *A23*) to *B.23*
- pin H8 ( *A24*) to *B.24*
- pin B6 ( *A25*) to *B.25*
- pin B4 ( *'CE'*) to *B.26*
- pin C6 ( *'WP'*) to *B.27*
- pin D4 ( *'RST'*) to *B.28*
- pin E6 ( *CLK*) to *B.29*
- pin F6 ( *'ADV'*) to *B.30*
- pin F7 ( *WAIT*) to *B.31*
- pin F8 ( *'OE'*) to *B.32*
- pin G8 ( *'WE'*) to *B.33*
- pin *F2* ( *DQ0*) to *B.34*
- pin *E2* ( *DQ1*) to *B.35*
- pin *G3* ( *DQ2*) to *B.36*
- pin *E4* ( *DQ3*) to *B.37*
- pin *E5* ( *DQ4*) to *B.38*
- pin *G5* ( *DQ5*) to *B.39*
- pin *G6* ( *DQ6*) to *B.40*
- pin *H7* ( *DQ7*) to *B.41*
- pin *E1* ( *DQ8*) to *B.42*
- pin *E3* ( *DQ9*) to *B.43*
- pin *F3* ( *DQ10*) to *B.44*
- pin *F4* ( *DQ11*) to *B.45*
- pin *F5* ( *DQ12*) to *B.46*
- pin *H5* ( *DQ13*) to *B.47*
- pin *G7* ( *DQ14*) to *B.48*
- pin *E7* ( *DQ15*) to *B.49*

11. The next column, **Type**, is optional for this example part. However if you should take interest in one of CADSTAR's Signal Integrity Verification (SIV) or Power Integrity Advanced applications, proper pin type declarations will be needed.

    Simply double click in the cell to reveal the list of available pin types and make your selection.

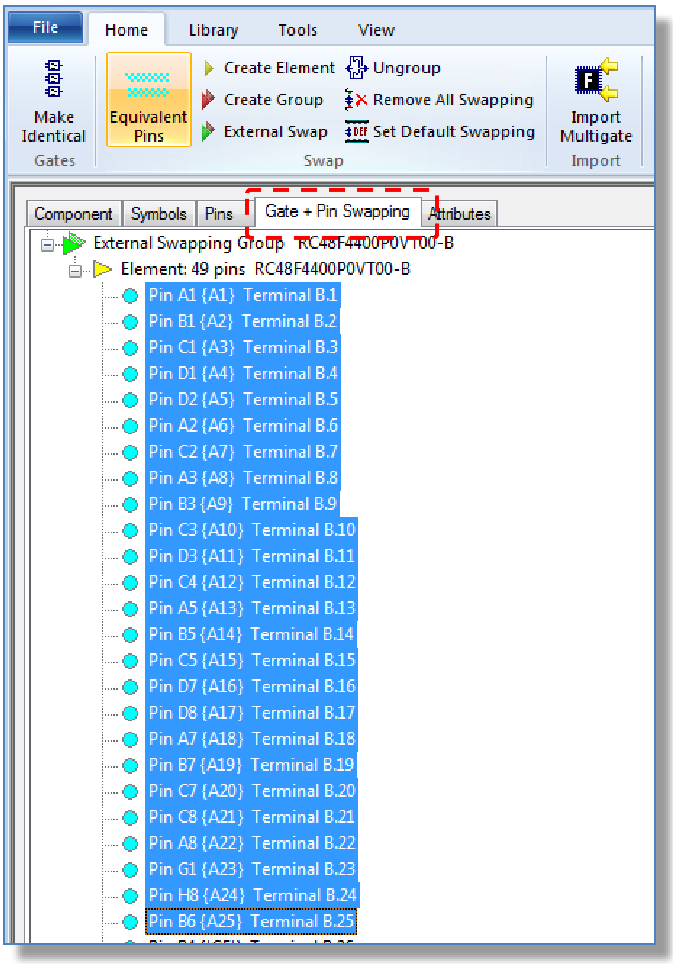



12. Select the **[Home]** tab and then select the **Gate + Pin Swapping** tab.

    Click to expand the External Swapping Group element containing 49 pins then expand the element contained within.

    Select the pins with the labels *{A1} – {A25}* as shown and click on the **Equivalent Pins** button or select <**R.M.B**.> → **Equivalent Pins**.

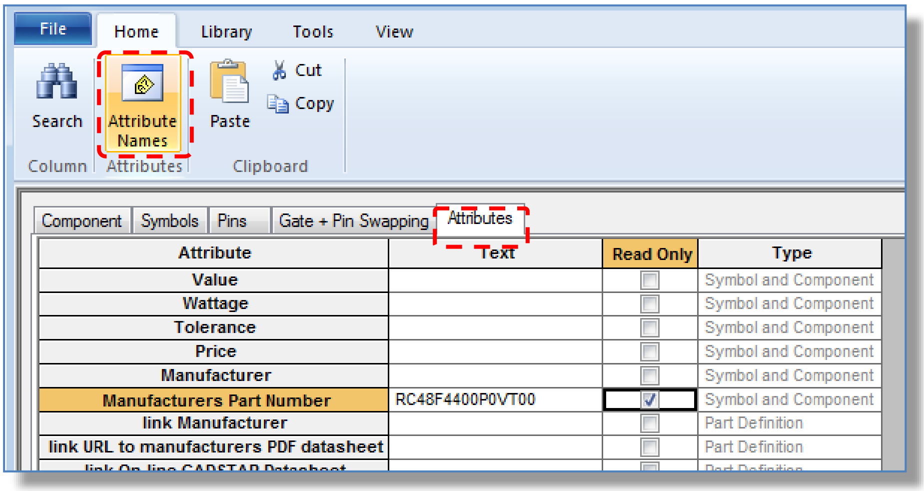
    Repeat the action for the pins with the labels *DQ0 – DQ15.* If you do so it will help you to optimize the routing pattern in the Design Editor and/or P.R.Editor XR.



13. Select the [**Attributes**] tab and click on the text field for **Manufacturers Part Number**. Add the value **RC48F4400P0VT00**.

    You can fill in more attributes if you like. Attribute values can be set as *Read Only* so users can not change their values in a design.

    **Tip:** You can create user-defined attributes by clicking on the **Attribute Names** button.




If you finished adding a part click on the [**File]** tab→ **Save** and **Close** the file.

If you didn't manage to add the part without errors or warnings you can browse the Library folder **..\...\Zuken\CADSTAR Express XX.X\Library** and delete the **Parts.lib**. Then rename the file **Parts_CS.lib** to **Parts.lib** and then select **Libraries→ Parts** and select **[Parts Index].** You should not have any errors or warnings.

## Congratulations on creating your first complex part in CADSTAR!

## Why not try and add it to a sample schematic?

## CADSTAR FPGA

If you want to skip most steps as described above you can also use a CSV (Aldec FPGA Data) file.

To learn more you can check out **CADSTAR FPGA**, supporting Actel, Altera, Lattice, Quicklogic and Xilinx flows from one universal project manager that controls all the design files for simulation, synthesis, place and route and pin assignment to the PCB.

Pin synchronization is often far from optimal for PCB routing; this new integrated solution supports the I/O synchronization between the FPGA device and the PCB board. CADSTAR FPGA supports forward- and back-annotate pin assignment changes in order to optimize PCB routing.

If you require any support during evaluation, please contact your local CADSTAR distributor.

Where to Buy CADSTAR

# Chapter 4 – Design C (Standalone Place & Route Editor)

Design C has been created for the more advanced users, allowing you to make use of the Standalone Place & Route Editor XR2000. Power Users of CADSTAR tend to prefer the more powerful features such as those available within the Standalone P.R.Editor XR2000, which provides placement and routing functionality and much more. By the way, all exercises completed for Design A and Design B in the Embedded Place & Route solution, can as well be designed in the Standalone Place & Route Editor XR2000!

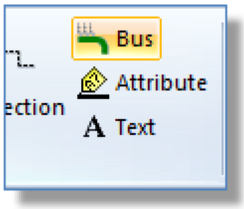
Also in this design we will learn how to create an Intelligent Bus and the use of Signal Reference Links.

## Step 1 - Schematic for Design C

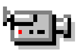
1. The schematic of Design C is provided and is nearly completed. Just open **DesignC_CS.scm** and save it as **DesignC1.scm** and begin.

   CADSTAR is capable of creating intelligent busses; you can restrict the signals connecting to a bus according to the signal names. The *Item Properties* dialog for a bus contains a [**Signal**] tab where connections to a bus can be defined. If you set a bus to be *none-restrictive* you can connect any net.

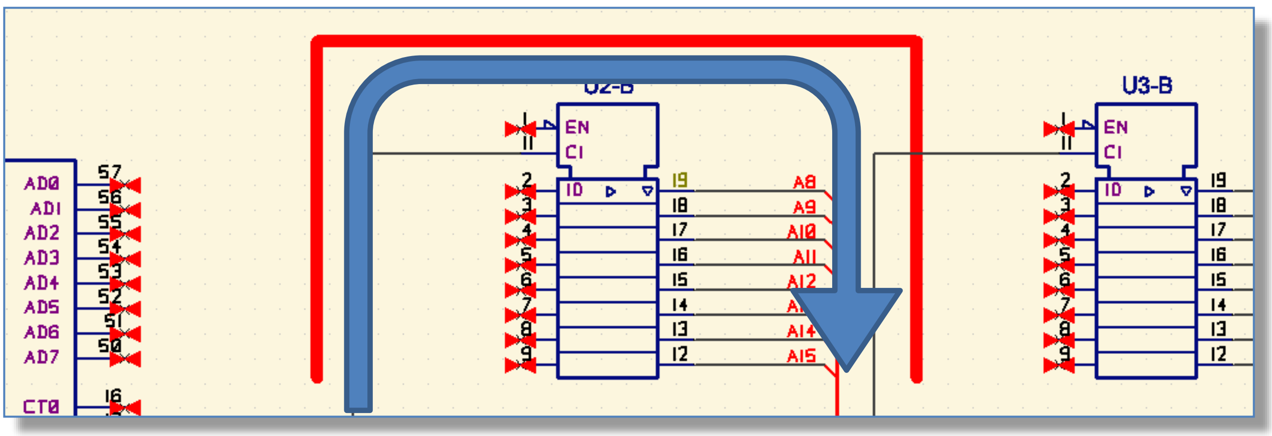
   Signal reference links are used to view and 'jump' to the other signal references of the same net throughout the (hierarchical) design.



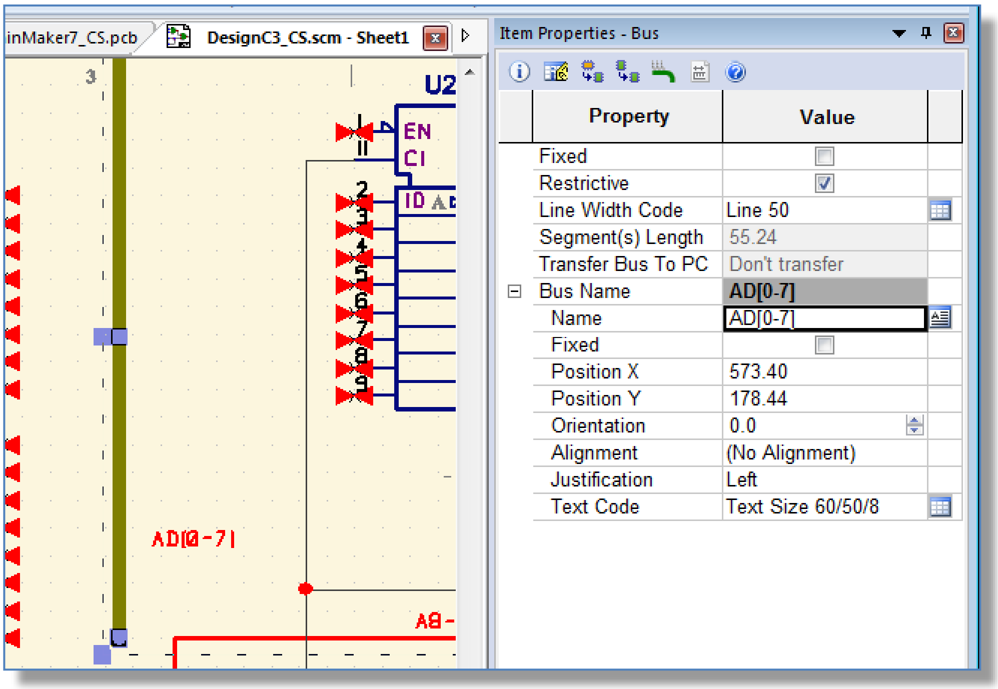

2. Select the [**Home**] tab and then select Bus.
   We will start by creating an intelligent address (AD0-7) bus on sheet 1 between U1, U2 and U3.



   Select the start point for this bus and draw the bus. To insert a corner click left mouse button, to finish the bus double click the left mouse button.



3. To add the bus name and signal names to the bus, select the bus and click the non-modal Item Properties panel. Fill in the bus name AD[0-7]

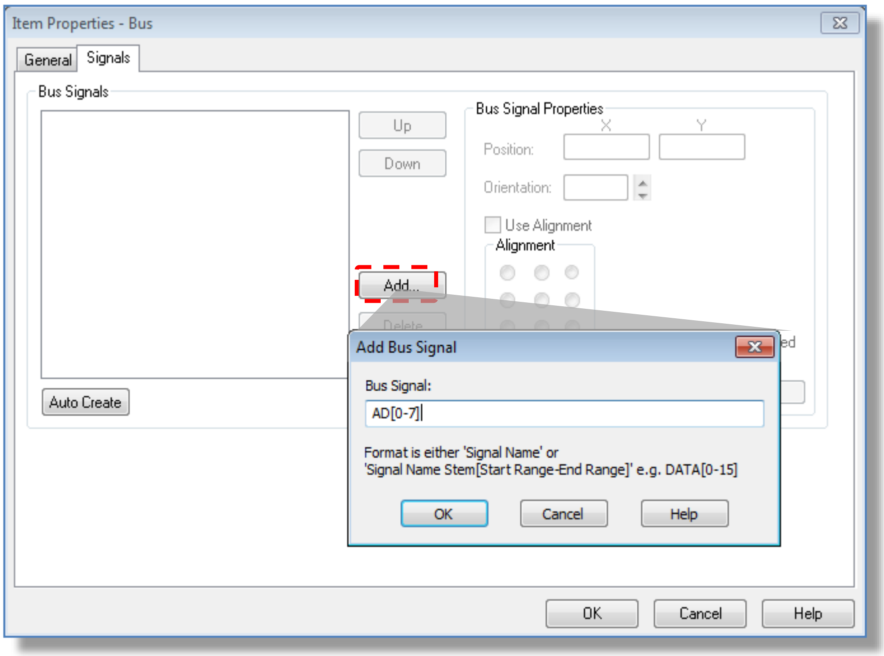



Alternatively this can be performed using the standard Items Properties dialog for Bus Items. With the Bus item selected click the <**R.M.B**.> and click **Item Properties**.

Select the **[Signals]** tab, click on **Add** and fill in ***AD[0-7]*** then press OK.

Click [**OK**] to exit the dialog.

You can now connect connections to the bus.

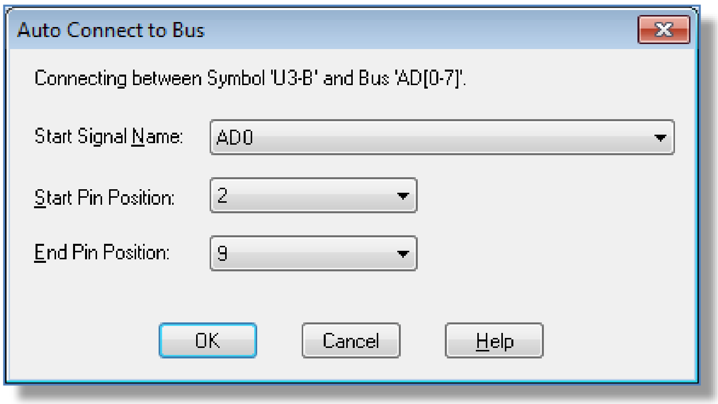


4. Select U3-B select the **Move** icon and move U3-B towards the bus until the terminals are on top of the bus, drop U3-B by pressing the left mouse button, the next window pops up

Set this window as follows:
Start Signal Name: AD0
Start Pin Position: 2
End Pin Position: 9
Press OK.

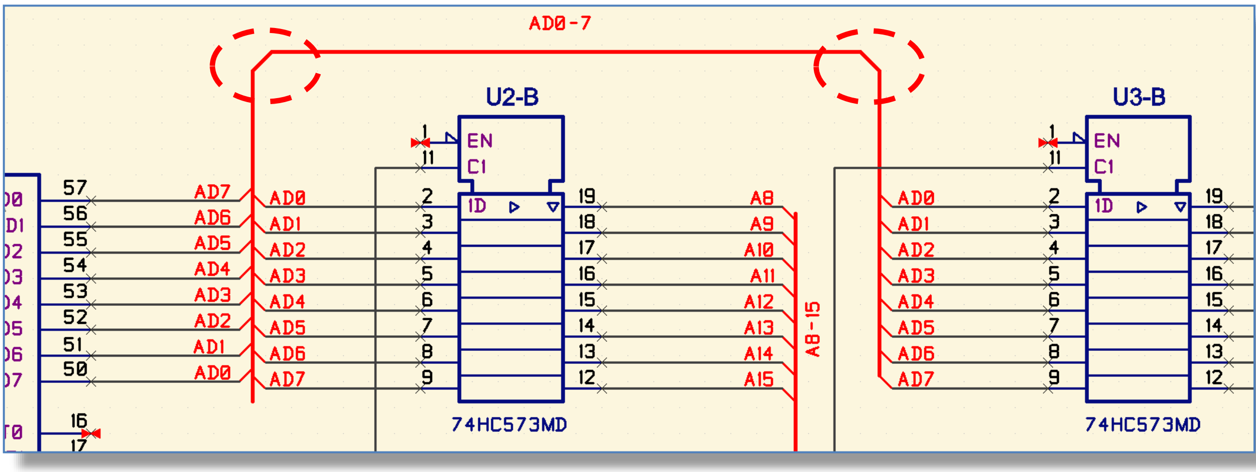
Move U3-B back to its original position.

Repeat this with U2-B.

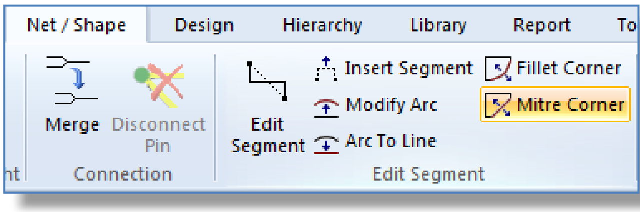



For U1-B:

Start Signal Name: AD0
Start Pin Position: 50
End Pin Position: 57
Press OK




**Tip:** Add Mitres to the bus corners using the **Mitre Corner** function located on the [**Net/Shape**] tab.

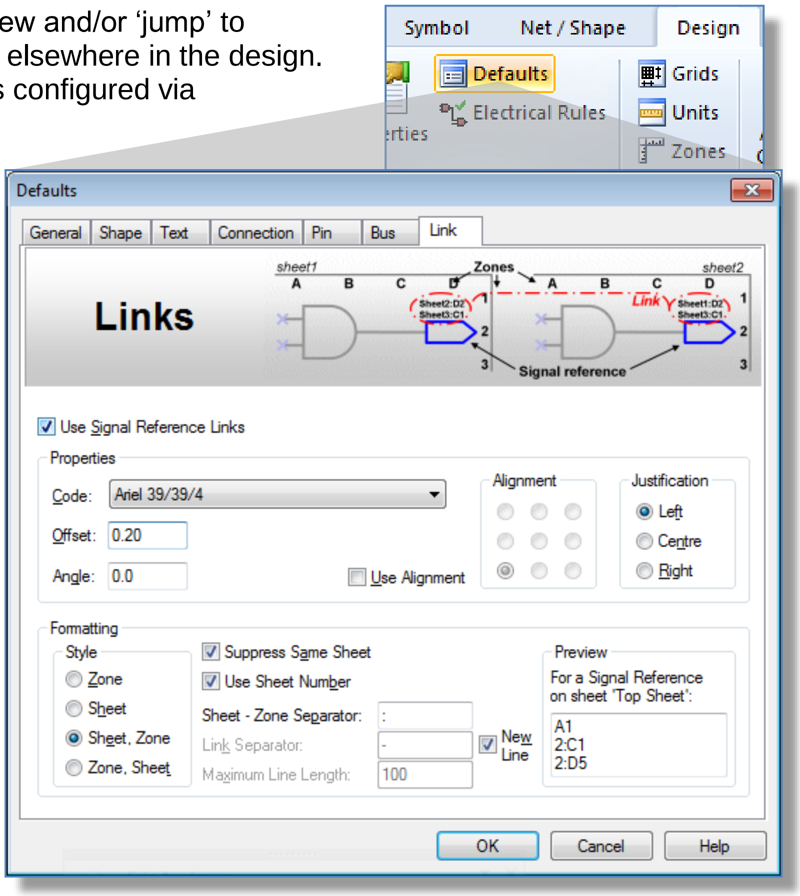



**Tip:** Bus Terminals can be rotated to suit the direction of the signal flow. Using the <**Ctrl**><**L.M.B.**> method select all of the bus terminals you wish to rotate. Once selected, use the rotate command of <**F3**>.

5. To connect single connections to the bus use the **Add Connection** function. Start at the pin to be connected, then drag the wire to the bus and single click to finish. The function will ask which signal name to add.

## Adding Signal Reference links.

Signal reference links are used to view and/or 'jump' to another associated signal reference elsewhere in the design. The visibility and format of the link is configured via the **[Design]** tab→**Defaults** dialog under the **[Link]** tab.




Zones configuration is controlled via the **[Design]** tab→**Zones** *dialog,*

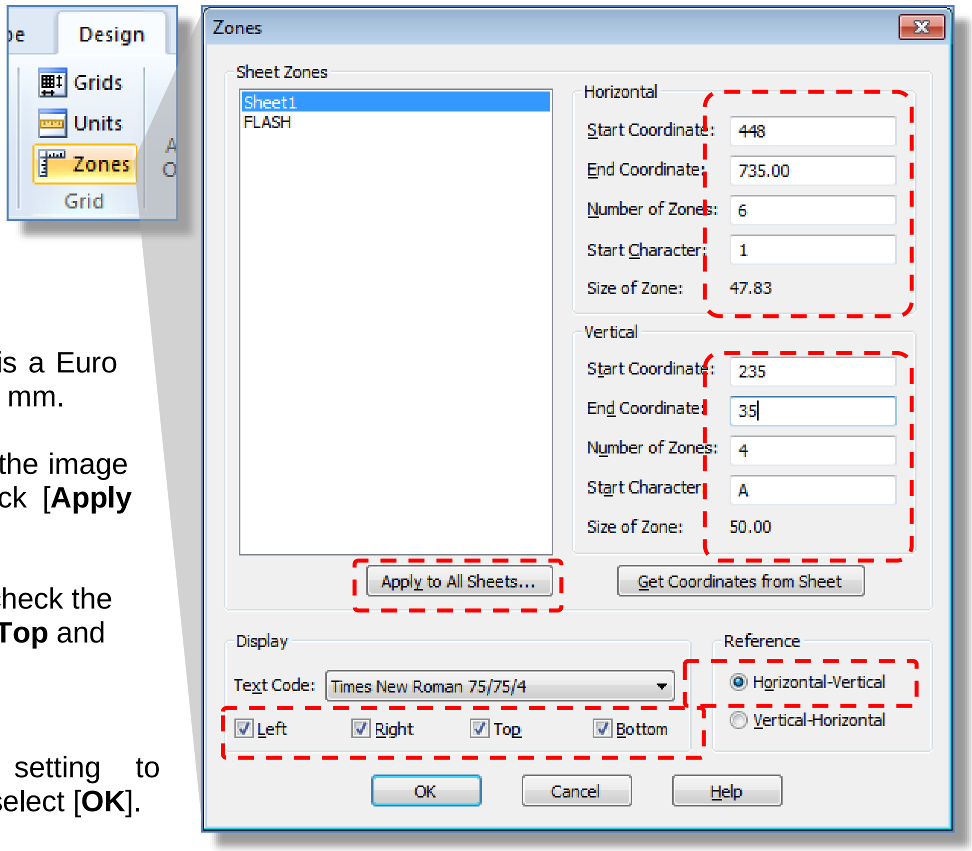
To specify the location of the link, zones can be used to split the sheets into horizontal and vertical segments.

6. Since the format sheet is a Euro size, change the units to mm.

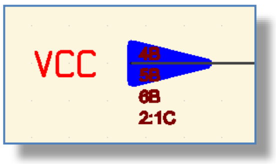
7. Set the dialog to match the image shown → and then Click [**Apply to all Sheets**]

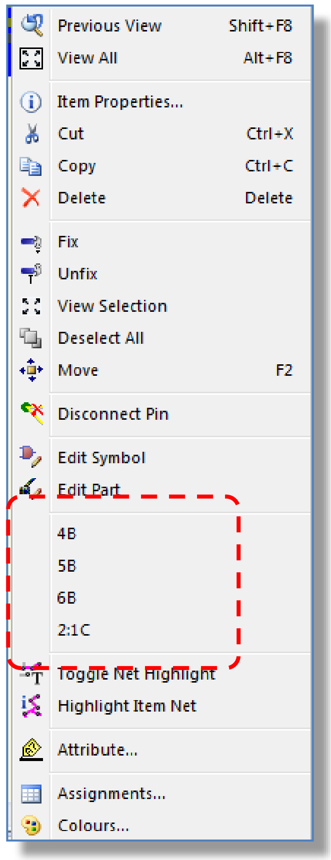
   In the **Display** section, check the options **for Left, Right, Top** and **Bottom.**

8. Set the **Reference** setting to Horizontal-Vertical and select [**OK**].



9. Now check the signal reference VCC in the lower left corner of the sheet. It should look like this:




You are now able to jump to the several VCC reference links in this design by double clicking on for example 1:6B or by selecting the Signal Reference then pressing the right mouse button and selecting one of the reference links. ➔

10. Save the schematic as DesignC3.SCM

    If you don't see the Signal Reference Links, just open **DesignC3_CS.scm** and save it as **DesignC3.scm** and then have a look.

11. Transfer the schematic to PCB through **[Design]→Transfer to PCB** as **DesignC1.PCB**, choose '*Eurocard-160x100.pcb*' as PCB technology.

    If you didn't manage to transfer the schematics design, just open **DesignC1_CS.pcb** and save it as **DesignC1.PCB** before going to step 2.

## Step 2 – Placement for Design C

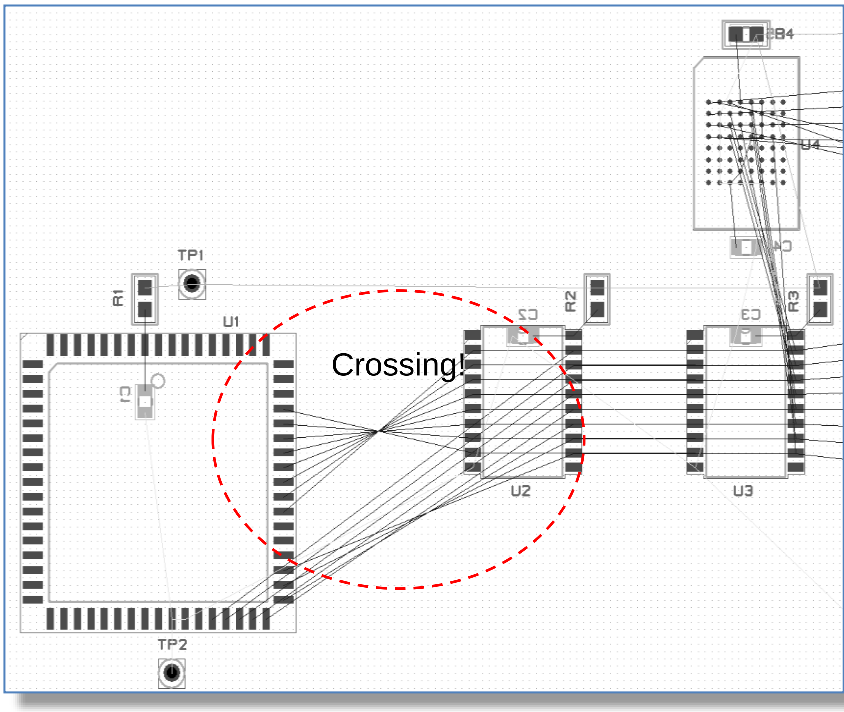
12. Create a rough manual placement here in the Design Editor.

Place all ICs as shown. →

SMD components can be placed on both sides of the board.

Place all the capacitors on the solder side of the board. I.e. Select capacitor C1 and drag it to the preferred place, click the <R.M.B.> and select '*Mirror*' from the *assist* menu and then single click to release.

**Note:** The colour of components when swapped to the other side of the board do change!

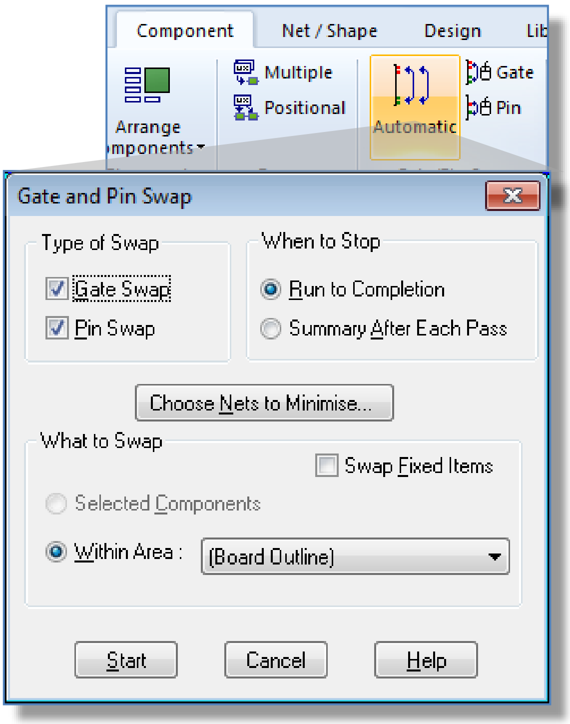



X1 can be placed at X 154.711 mm, Y 89.383 mm and rotated to 90 degrees.

If you didn't manage to place the components, just open **DesignC2_CS.pcb** and save it as **DesignC2.pcb** and then continue.

**Tip**: to see highlighted nets that connect to a component, press "**T**"<**enter**> on the keyboard to toggle the associated nets to a highlight colour.

13. Some connections between U1 and U2 are crossing! To solve this, select the **Automatic Gate and Pin Swap** button on the **[Component]** tab and click **[Start]** .




Save the design as **DesignC3.pcb**

**Note:** You can also swap pins on the fly in the Standalone Place & Route Editor XR2000.

Using CADSTAR you can decide to use schematics as master or the PCB design as master. CADSTAR supports full back annotation. No matter what your choice will be, do not forget to run a **Back Annotation** when you have changed something in your PCB design, like pin and gate swap, renamed components, added, modified or deleted components, connections or attributes.

If you didn't manage to do Gate and Pin Swap, just open **DesignC3_CS.PCB** and save it as **DesignC3.pcb** before going on.

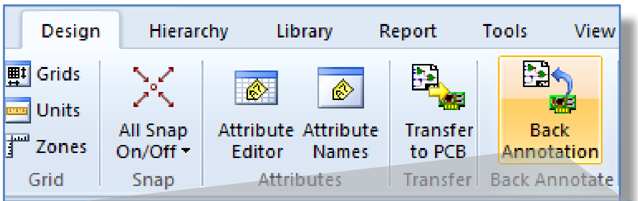
14. Open the schematic design **DesignC3.scm** and select **Back Annotation** located on the **[Design]** tab.

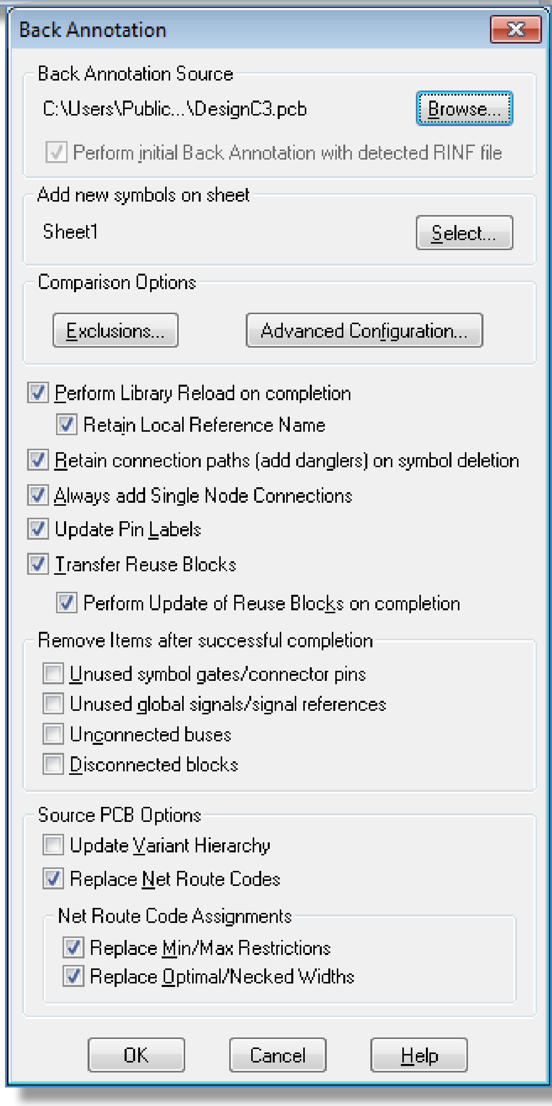
    In the ***Back Annotation*** window select the PCB design **DesignC3.pcb** as the source.

    If you have added new components in the PCB design that do not exist in the Schematics you can select the sheet on which you want to add these components (in this case just select *Sheet1*).

    The exclusion file can contain components that do not exist in the schematics, like mechanical holes or other components that you don't want to appear in the schematics. Just select ***Example3.cig***.

    Now select **[OK]** to run the back annotation.

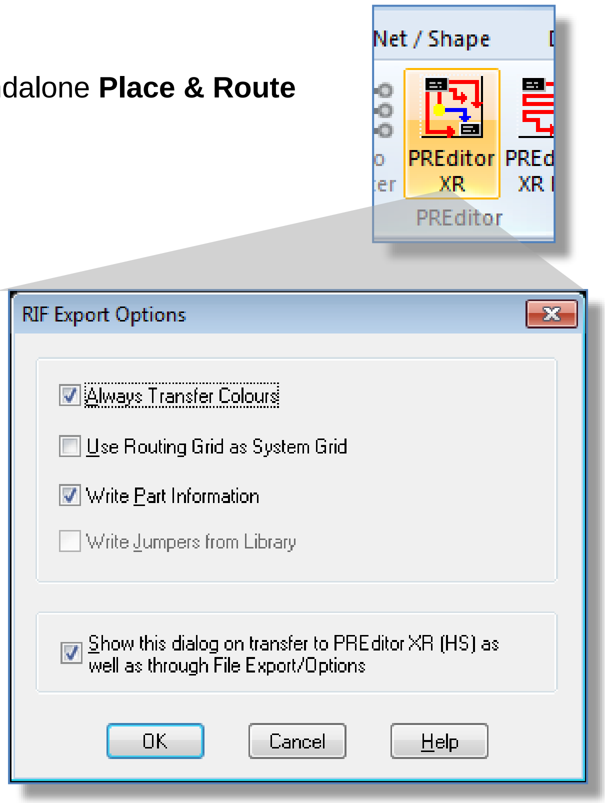


CADSTAR

## Step 3 - PCB Routing for Design C

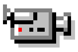
1. Continue with **DesignC3.pcb** and go to the Standalone **Place & Route Editor XR** by selecting **Tools→PREditor XR.**




When transferring to the P.R.Editor a *RIF Export Option* window will be showed automatically.

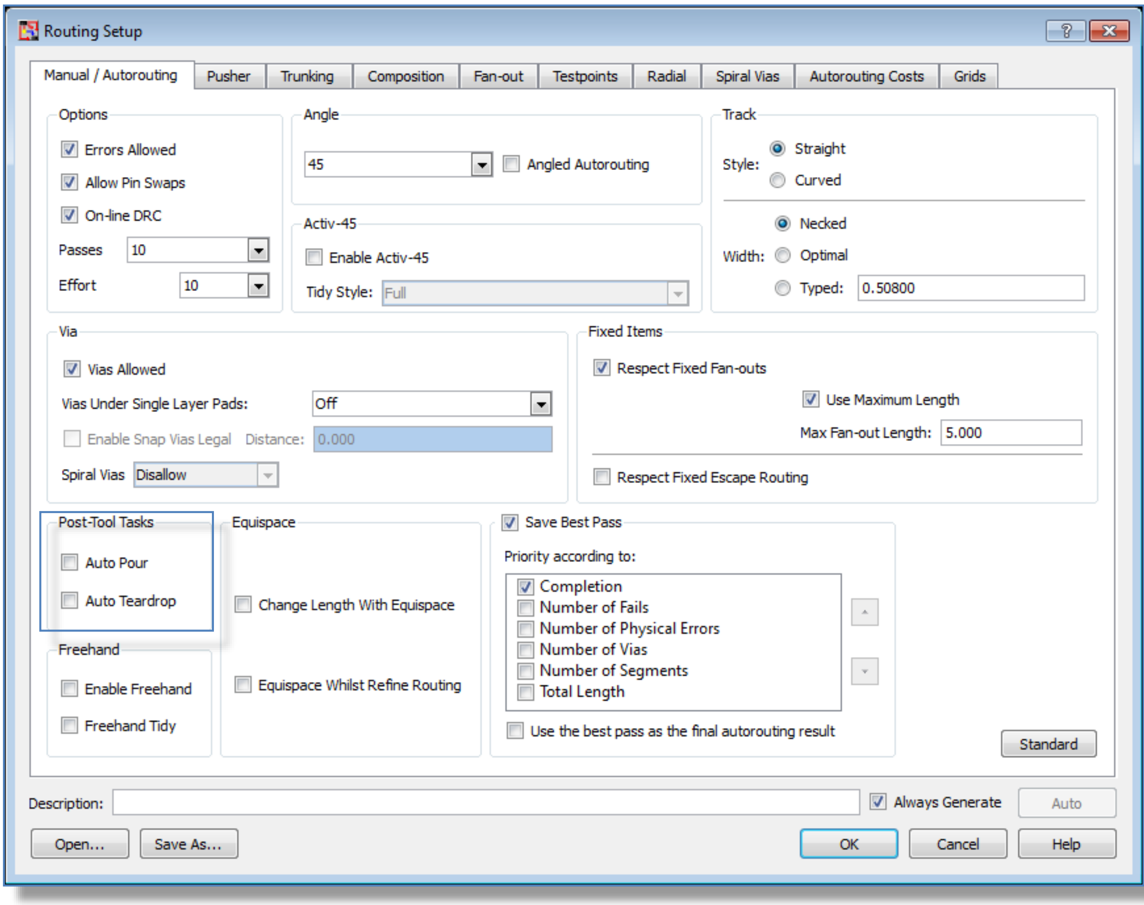
Be sure to enable **Always Transfer Colours**.

Click **[OK]**



Before starting any routing or further placement check the **Configure→Routing Setup** dialogs or (CTRL-T).

Setting the routing options is very important before any routing. Ensure the settings are equal to the example shown below. {If you don't like copper to be poured automatically disable **Auto Pour**} {values are shown in mm.}

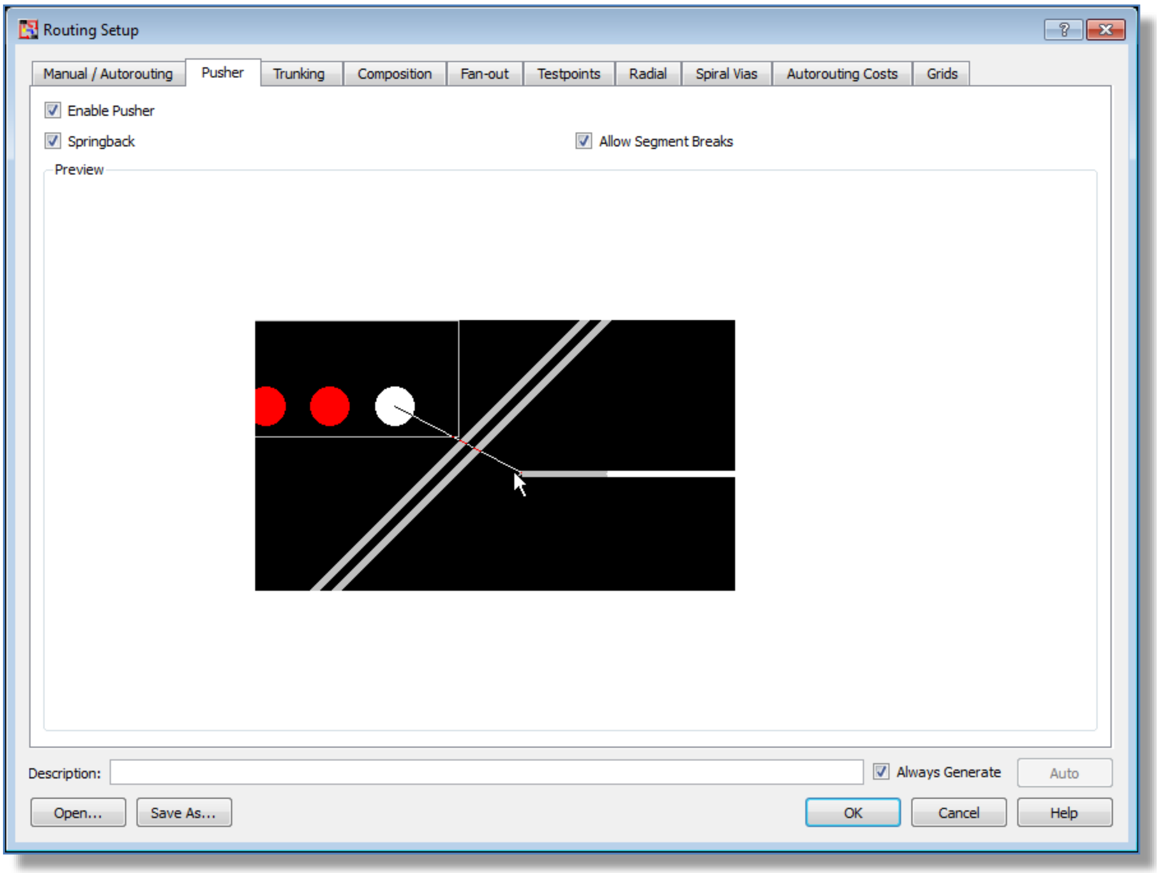




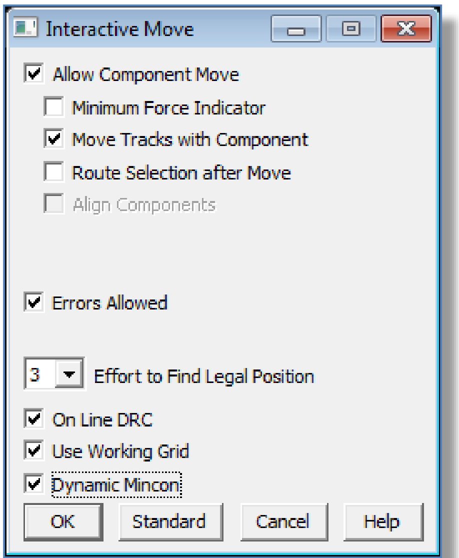



ZUKEN

If you don't like routes to be pushed by other objects you can disable the **Pusher.**



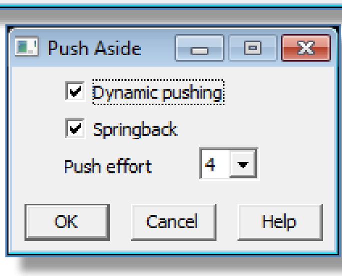

P.R.Editor can also be used for placing components without going back to the Design Editor. Before starting any placement check the **Interactive Move** and **Push Aside** options.




2. Set the options for moving components by selecting **Configure→Interactive Move** in the menu bar.

Setting the placement functions behavior is very important before any placement is started.

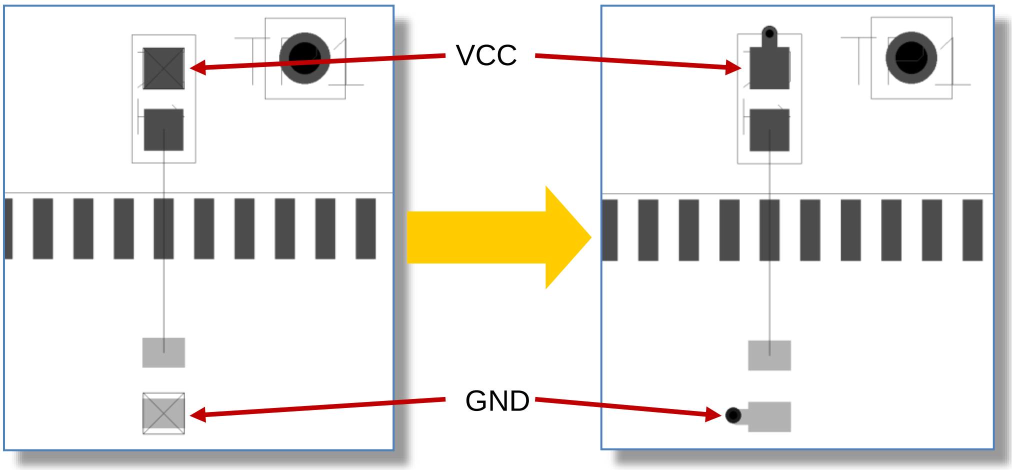
3. Select **Configure→Placement→Push Aside** in the menu bar. Ensure the settings are equal to the example.



4. Select a component and click the **Move** tool bar icon . Notice that other components are being *pushed aside* and when there is enough space the selected component jumps over other components. Components can also be swapped to the other side of the board or rotated This can also be performed using the **<R.M.B.>** assist menu.

As this board is a 6 layer board with 2 power planes GND & VCC, we will first start with stub routing for the GND & VCC.

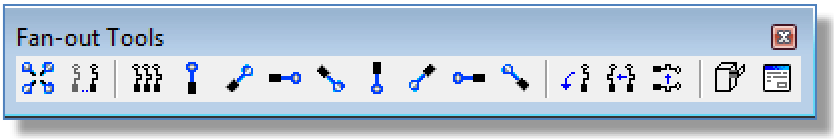
5. Select **Whole Net Mode** , **Auto route** and select the GND signal at a pin location (repeat the same for VCC).




The Place & Route Editor XR will help you in routing your designs by using several auto-routing technologies on a single net, a group of nets or within a certain area.

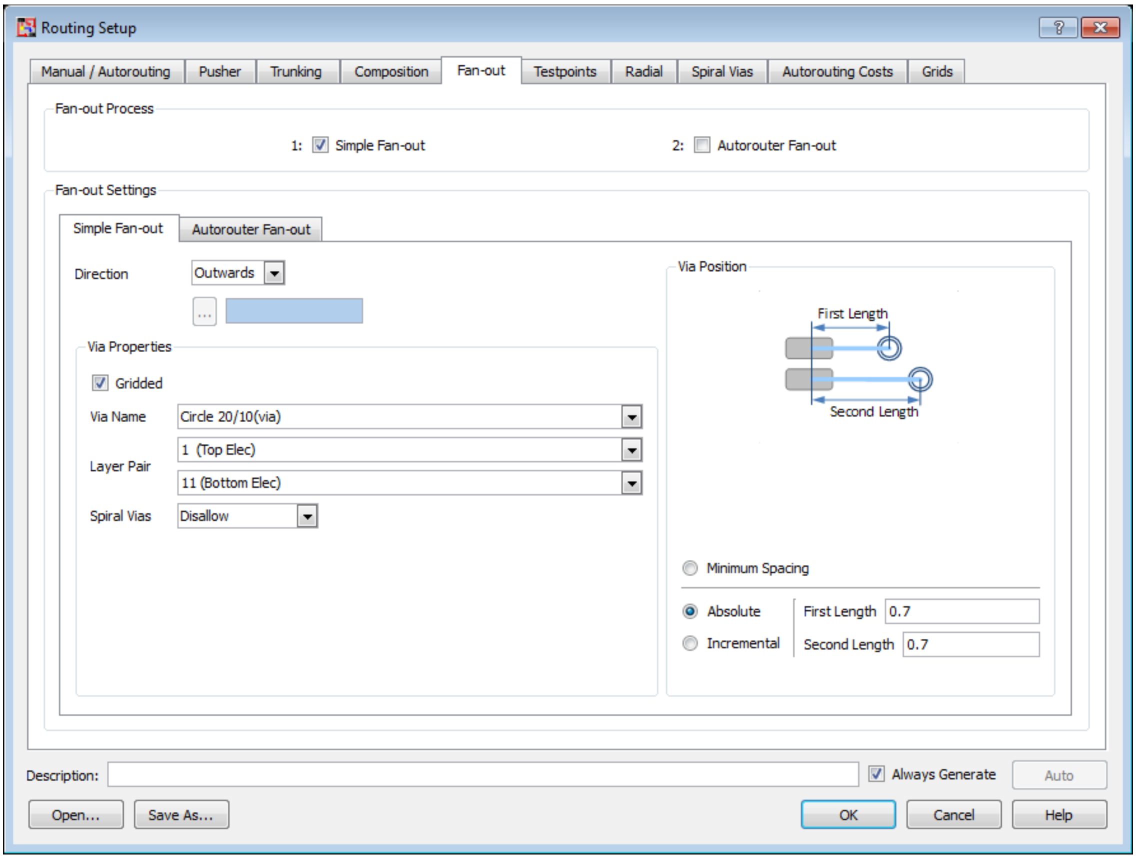
**Note*:*** By using the customizable *Function Keys F5 or F6* you can scroll through the layers from top to bottom or the other way around (Try it).

6. The next step is to create a Fan-out for a BGA. A Fan-out is a route template that can be applied to an SMD component. It enables routes to `breakout' from a surface mounted pad using a pattern that is efficient on space and gets the route to an inner layer as soon as possible. Fan-outs are often used and can be easily re-used for BGAs, QFPs or other devices.




***Note:*** If the Fan-out toolbar is not visible go to **View→Toolbars→** select **Fan out.**

7. Before creating the actual Fan-out, select **Configure→Routing Setup [Fan out]** tab - ensure the settings are equal to the example shown below.

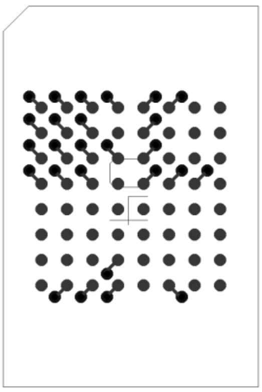



8. Select **Configure→Routing Setup→[Manual/Autorouting]** tab and change the Width from *Necked* to *Typed* and enter a value 0.157 mm.

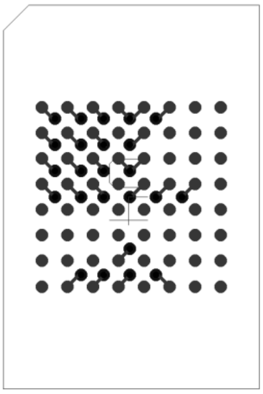
**Note:** If your Units are set to Thou., as indicated at the bottom of the Place & Route Editor window, double click on the unit shown and change it to Millimetres with 3 decimals for precision. Suggested Routing and Via grid for mm should be 0.1. See **Routing Options** dialog [**Grids**] tab.

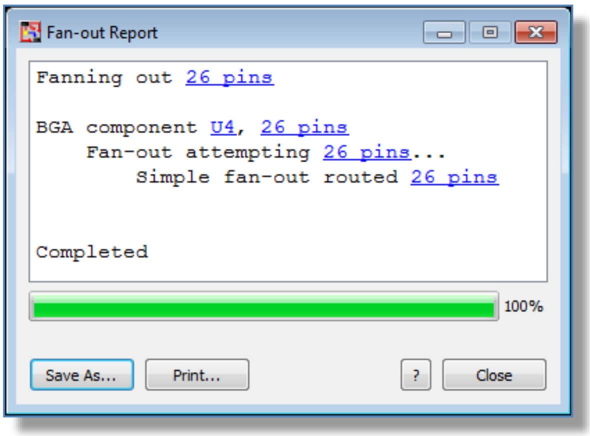
9. Select **Routing→Fan-out→Perform Fanout** in the menu bar and click to frame an area around the component U4 (bga64) or just a number of pads.

Outwards



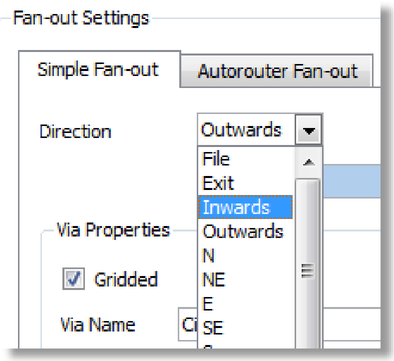
Inwards






(HTML Fan-out report dialog)

If you would like to change the direction of the fanned out traces from Outwards to Inwards, select **Configure→ Routing Setup** [**Fan-out]** tab and change the direction from Outwards to Inwards.



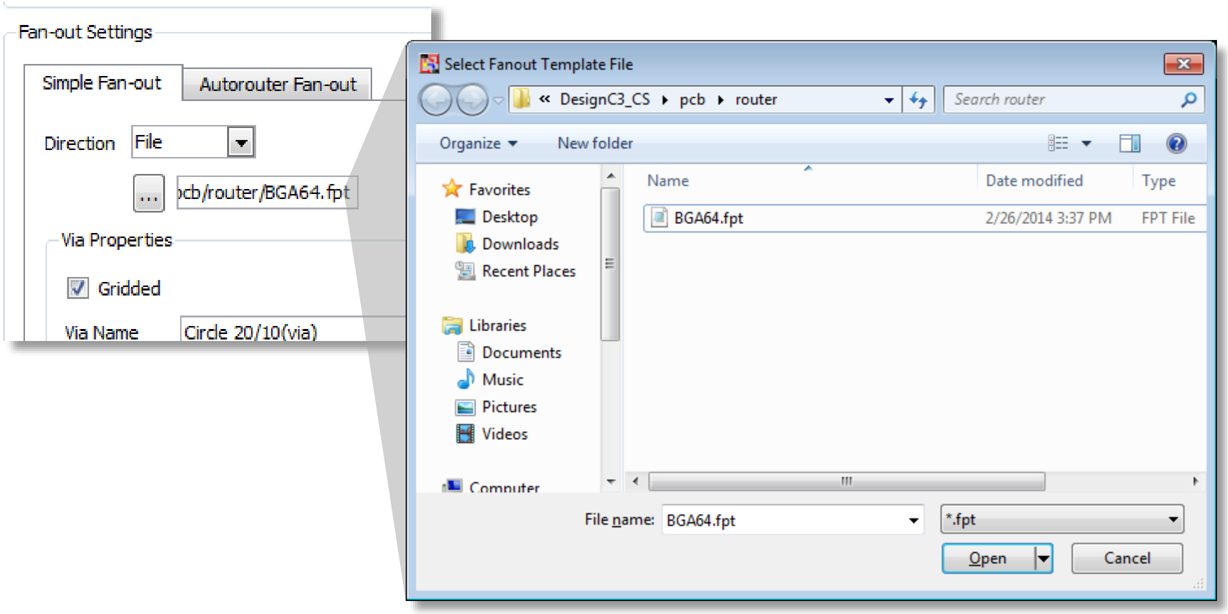

Select the **[OK]** button on the menu and Undo the previous Fan out.

Select **Routing→Fan-out→Perform Fan out** in the menu bar and click to frame an area around the component U4 (bga64) or just a number of pads. This time the pattern should be opposite.

10. When you are happy with the Fan-out you can save it for reuse, by selecting **Routing→Fan-out→Save** (located on the Fan-out tool bar) and click to frame an area around the created Fan-out, so you can re-use it within other designs. Save the Fan-out as 'bga64.fpt'.

Zoom-in on component U4 and *Unroute* the created Fan-out.

11. Select **Configure→Routing Setup** [**Fan-out]** tab and change the direction to **File**. Click the file browse button and open the file **bga64.fpt**.




Select the **[OK**] button on the Routing Setup dialog.

Undo the previous fan out.

12. Select **Routing→Fan-out→Perform Fan out** in the menu bar and click to frame an area around the component U4 (bga64) or just a number of pads. This time the pattern will come from the fan out file.

**Tip:** Once a design is fully “fanned out” the entire design can be saved to one fan out file. Each components’ reference shapes’ fanned out pin data will be saved. If the design ever needed to be rerouted using a different placement, the fan outs can easily be restored.

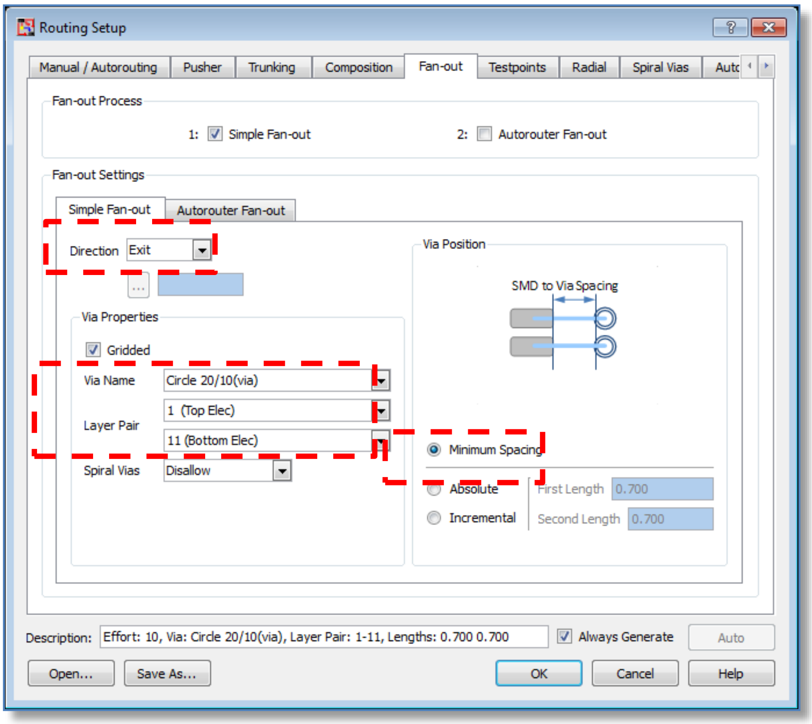
13. Select the **Configure→Routing Setup [Fan-out]** tab.

Set *Direction* to **Exit.**

Set *Via Position* to Minimum Spacing.

Set *Via Name* to **Circle 20/10(via).**

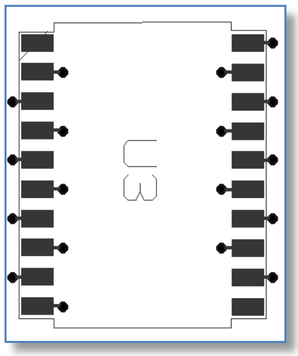
Set *Layer pair* as shown.




14. Select **Routing→Fan-out→Perform Fan-out** or click the icon located on the Fan-out tool bar and frame an area around the component U3.

This option uses the default pin exit directions for the various pad shapes as a guide to create the fan out entities.

This can be used on all SMD components to quickly and easily fan out an entire design.

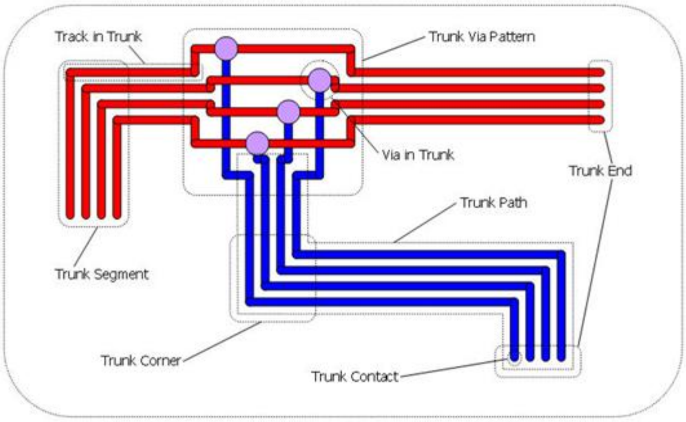


15. For the next steps continue with your design or open **DesignC4_CS.pcb** in the Design Editor, save it as **DesignC4.PCB** and then select **Tools→PR Editor XR**.

The Place & Route Editor XR will help you to complete your design step-by-step by using advanced auto-route technologies. For instance; ***Trunk Routing*** will help you to complete data and address lines easier.

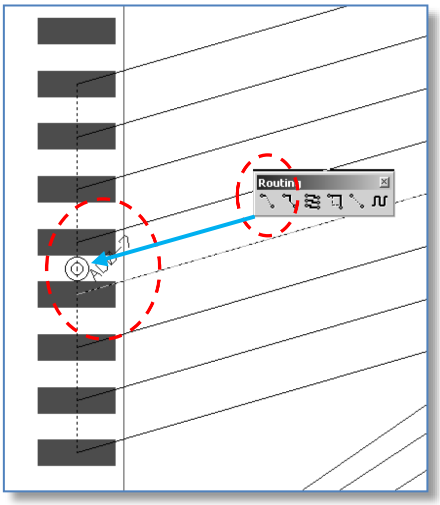
***What is Trunk Routing?***

Trunk Routing introduces the concept of the intelligent trunk object, allowing you to route any given set of signals in an intuitive manner and with as little effort as possible.



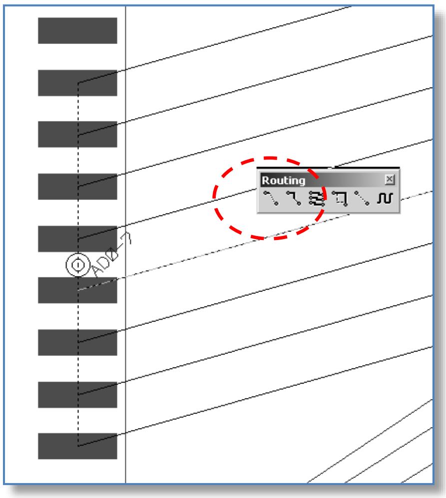

Trunk System

16. Selecting which connections are to be Trunk Routed.



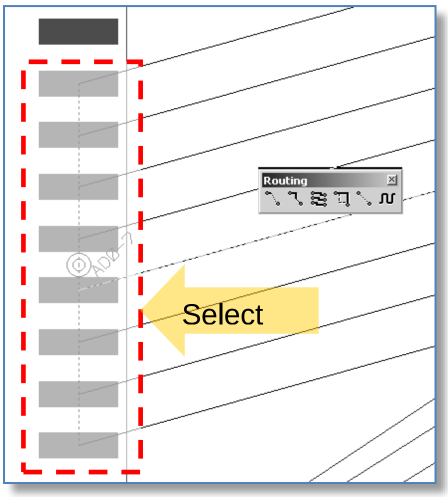

← Busses of data and address lines can be pre-designated in a schematic design (as done in DesignC) and transferred to PCB and Place & Route Editor XR. A named bus (trunk) can be selected by its' bus marker.

Zoom in on the bus marker. Select **Manual Route** and (Shift + Click) on the round marker. This will start the action.



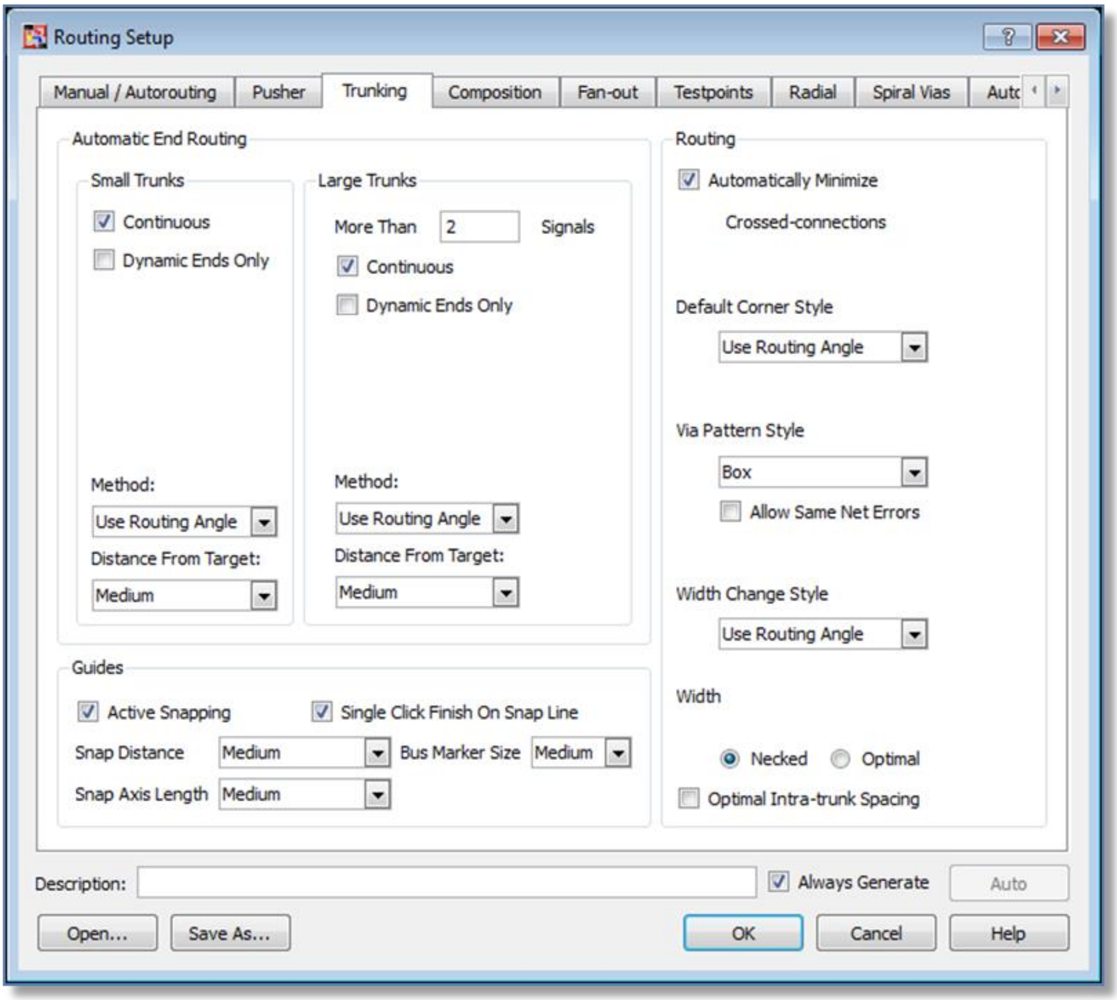

Alternatively you can double click on one of the pads as marked by the bus marker, before selecting **Manual Route** .

**Note:** All pads as marked will be selected and highlighted.




If bus signals have not been defined in the schematic, no bus marker will be visible. Alternatively you can drag a multiple selection around a set of pins or connection wires before selecting **Manual Route** to start Trunk Routing.

17. Before starting any trunk routing we advise you to check the Trunking Options located in the **Configure→Routing Setup [Trunking]** tab.




## Simple Manual Routing of a Trunk on a Single Layer

In order to aid routing, snap axes and trunk-end routing areas will be drawn on the canvas around each of the target sets of pins for the trunk. You will see ***Twist Arrows*** drawn on the canvas showing the best entry angle for the trunk to the target pins, this allows minimization of connections crossed at each end. You will also notice that you have a Gather Point for the trunk that is now dynamic on the end of your cursor. The *Gather Point* defines the start for the trunk where all of the parallel tracks will be considered as a single object.

18. To start routing the trunk you can place the Gather Point by clicking the left mouse button in the position that you want to start routing the trunk from. Trunk segments are now introduced towards the cursor position as you move the mouse on the canvas. Use the left mouse button to confirm trunk segments that you have added. A corner can be added by changing direction of movement of the cursor after a left mouse click.

**Note:** There are different styles of corners that can be added during trunk routing. This can be changed by using the Right Mouse Context Sensitive menu.

When you have added the required trunk path, it is possible to finish trunk routing in several ways:

- The ***'Escape'*** key can be used in order to finish trunk routing at the last added corner position or using the Right Mouse Context Sensitive menu ***Cancel*** option.

- With the ***'Single Click Finish on Snap Line'*** option selected on the ***Trunking Options*** dialog, a single click when positioned over a snap axis will also finish the trunk. Remember to select **Configure → Routing Setup →[Trunking]** tab in the menu bar.

It is also possible to restart the Trunk Router on a previously added trunk. This can be easily done by selecting the manual routing icon and then picking the trunk on the canvas, or selecting the manual routing icon with the trunk item already selected
**Note:** Try also the '***Backspace'*** key (remove previous Item).

During routing of a trunk, the trunk contents will dynamically reorder to maintain the least number of crossed connections at each of the ends. This is done to give the best routing pattern for each end. This option can be configured using the ***Trunking Options*** dialog ***Minimise Crossed Connection*** setting.

### 19. Adding Vias while Trunk Routing

To place a trunk via pattern while using the trunk router, you can double click the left mouse button or choose a different layer using the Layer option on the Right Mouse Context Sensitive menu. It is also possible to change the ***trunk via pattern style*** to a number of predefined styles using the Right Mouse Context Sensitive menu during trunk routing or by pressing the ***'Tab'*** key in order to cycle through the predefined trunk via patterns.

### 20. Manual Reordering of Trunks and Via Patterns

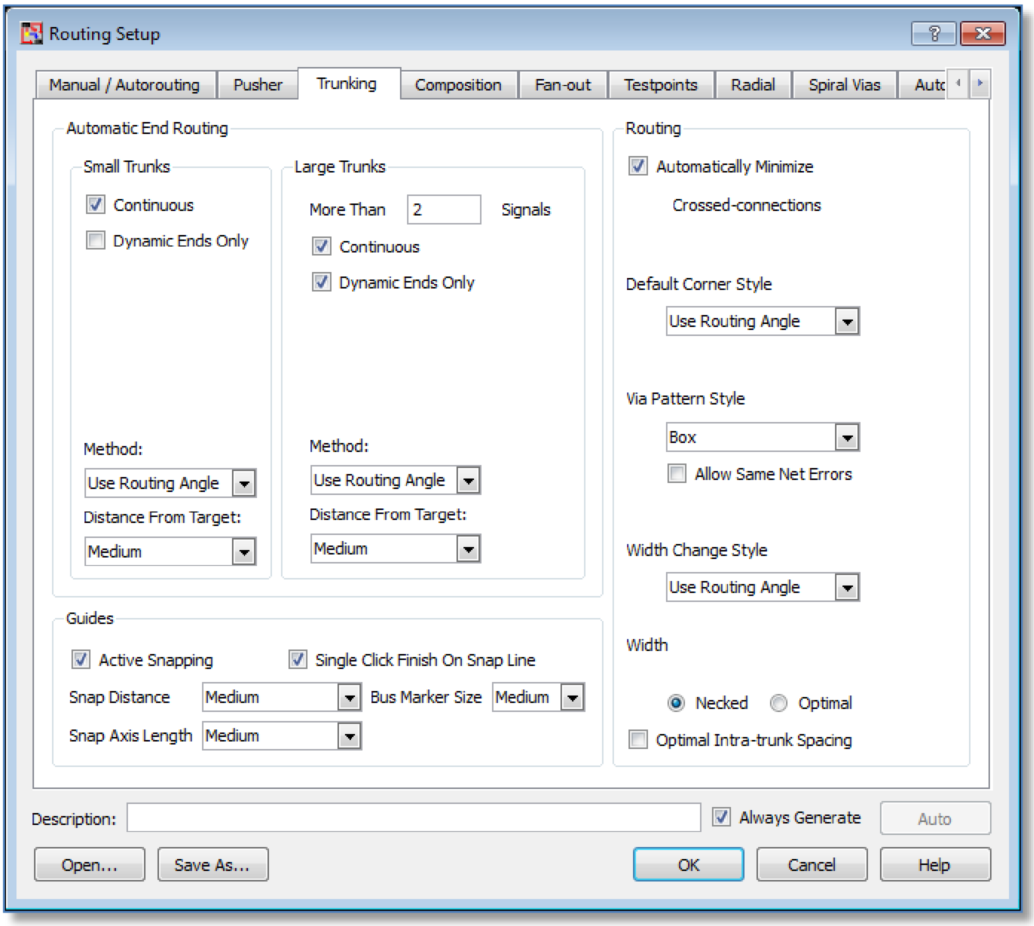
It is possible to reorder the contents of a trunk manually by select a single track segment inside the trunk. i.e. Hold down the ***'Shift'*** key and click the left mouse button to select a track. Choose one from the selection list. Hold down the <L.M.B.> and drag the track segment with in the trunk and watch how the selected segment appears to move from position to position. It is possible to switch to one of the other items by pressing the ***'Tab'*** key. Each time the ***'Tab'*** key is pressed the next segment closest to the cursor will be outlined. You can then drag this track to another position inside the trunk.

### 21. Manual Trunk End Routing

You can use the Manual and Activ-45 routers to interactively route the connections up to the end of the trunk. During the routing process you can still re-order the trunk if necessary.

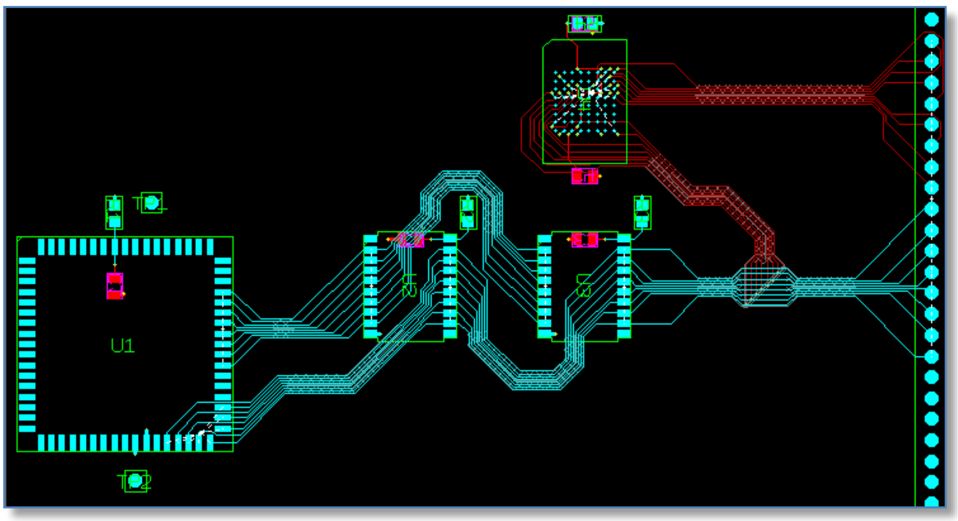
### 22. Automatic Trunk End Routing

While you are trunk routing, it is possible to automatically route the ends of a trunk using the trunk end router. Routing will be attempted for all trunk ends that are inside a trunk end routing target area. Select **Configure→Routing Setup→[Trunking]** *tab* and ensure the settings are equal to the example shown below.




In some circumstances you may wish to *decompose* trunk objects that you have added to your design into individual routes. For example, you may want to split a segment of a bus into routes so that you can route the bus around an obstacle. To do this, select the trunk items that you wish to decompose and then use the **Decompose** function on the **<R.M.B.>** menu.

**Note:** Once a trunk has been decomposed, it is not always possible to compose these items back into trunks. If they have been modified beyond their closest spacings you can use the



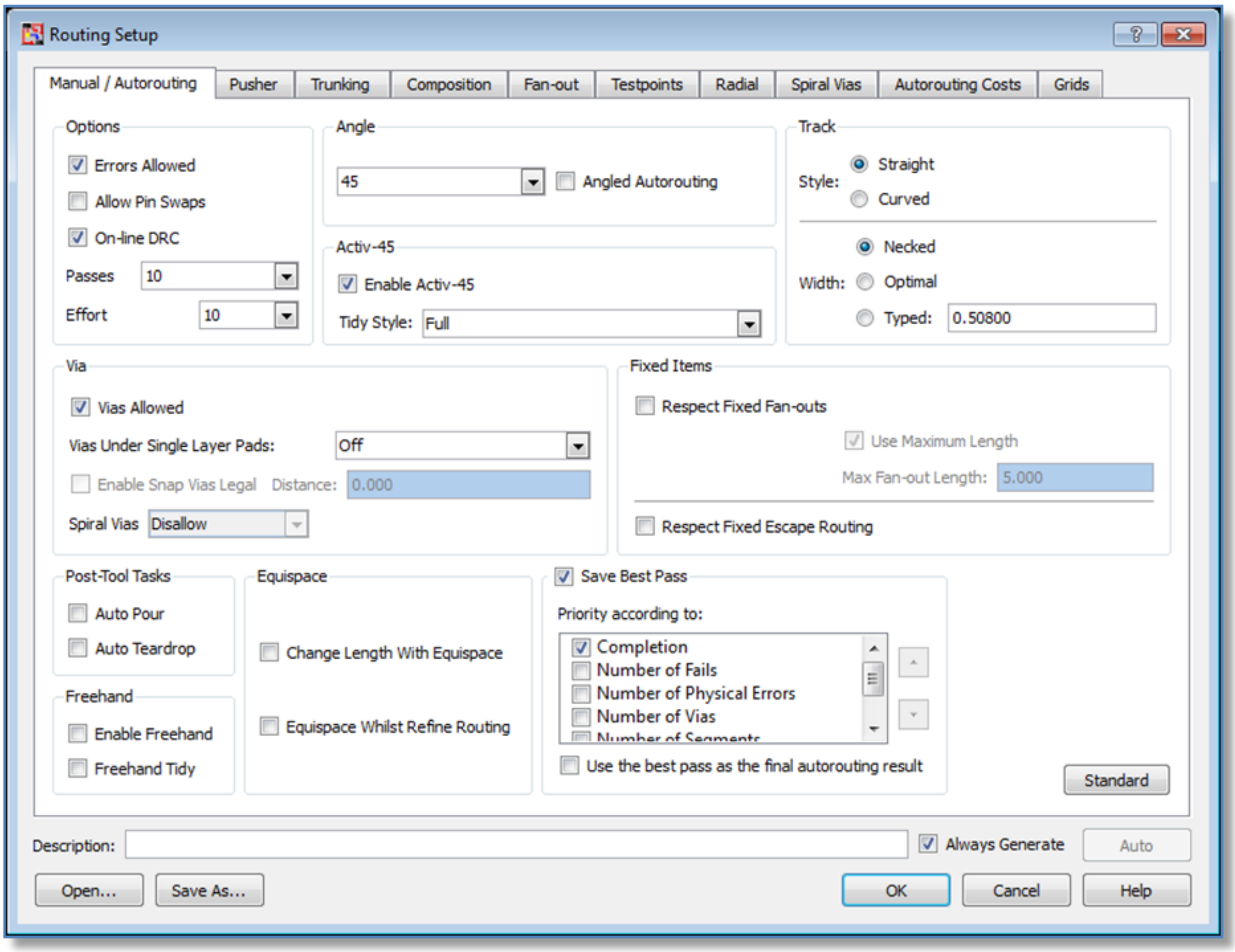
Trunk Routing, Manual and Activ-45 routers to interactively route the connections up to the end and finish the board.

If you didn't manage to complete the trunk routing then exit the P.R.Editor XR without saving and you will automatically return to the Design Editor and open **DesignC5_CS.pcb** and save it as **DesignC5.pcb** and continue.

## 23. **Auto Routing**

For the next exercise you should open **DesignC6_CS.pcb** and save it as **DesignC6.pcb** in the Design Editor and go to the P.R.Editor XR by selecting [**Tools]** tab**→PR Editor XR** . This design is not routed since it will be auto routed.

Before starting any auto routing, change the **[General] Routing Setup** options (CTRL-T). Setting them correctly is very important before any routing! Ensure the settings are the same as in the example shown.




***Note:*** Although errors are allowed, you should first allow the router to make some errors. In combination with Effort 10 the router will continue routing till no errors are left.

24. Select **Routing→Autoroute** from the menu bar and drag an area around the whole board outline or part of the board you would like to auto route. The auto router will stop automatically once all connections have been routed. The routing might not be optimal, and therefore you can run a Refine Routing Pass.

25. Select **Routing→Refine Routing** from the menu bar and drag an area around the whole board outline or part of the board you would like to refine.

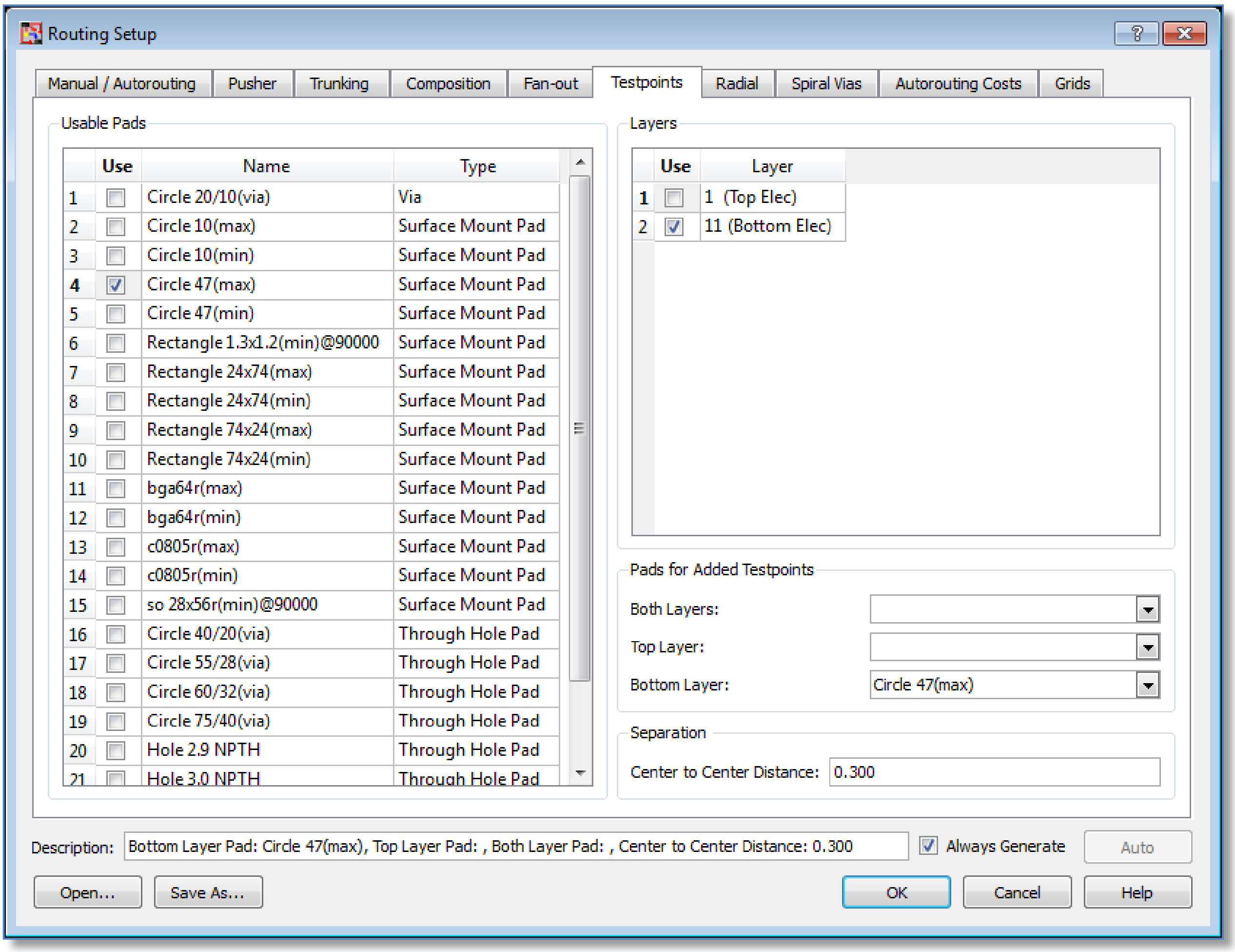
**Note:** As a result of the Refining Pass the number of vias and segments will be reduced.

26. Lastly, select the **Mitre** function located on the [**Routing**] menu and draw a frame around the entire board outline. This will change the 90° angles to 45°.

**Note:** you can mitre layers individually by turning the layer visibility off for layers that you do not wish to be modified.

If you didn't manage to complete the autorouting then exit the **Place & Route Editor XR** without saving. You will automatically return to the Design Editor where you can open **DesignC7_CS.pcb,** save it as **DesignC7.PCB** and then go to the P.R.Editor XR to for this step.

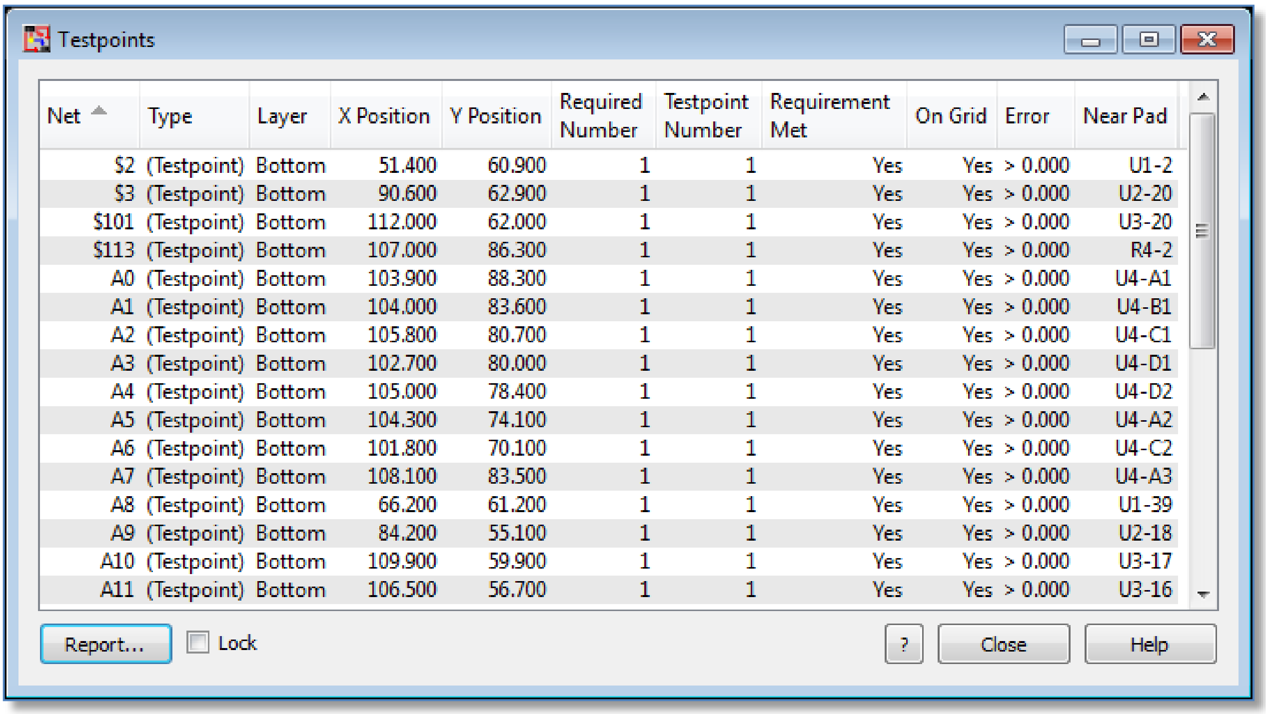
27. For In Circuit Test (ICT) purposes you can decide to automatically generate a testpoint on every node (or as many as possible). Before starting any allocation of testpoints, select **Configure→Routing Setup→[Testpoints]** tab and ensure the settings are equal to the example. Do not forget to select '(**Bottom Elec**)' in the Layers section option!




The settings shown on the previous page will use the surface mount pad **Circle 47** on the (max) *Bottom Elec* layer for every net. The link to the demonstration video will show the results of also including a through hole via as a usable test point option. Try the exercise both ways!

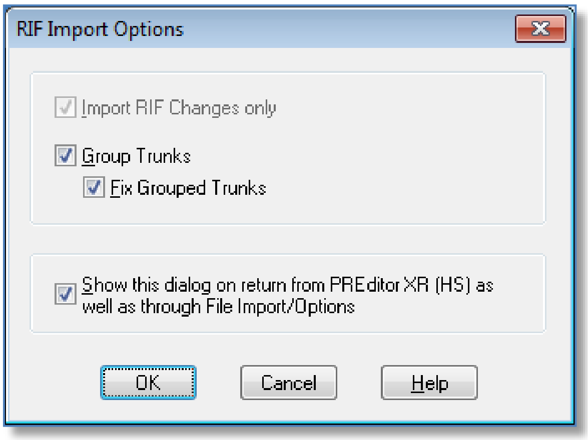
28. Now click on **Select→All** from the menu bar or you may use <**Ctrl+A**>, and all will be selected. Select **Routing→Testpoint→Allocate** and the testpoints will be added automatically.

29. Select **Utilities→Reports→Testpoints** to create a testpoint report as in the example.

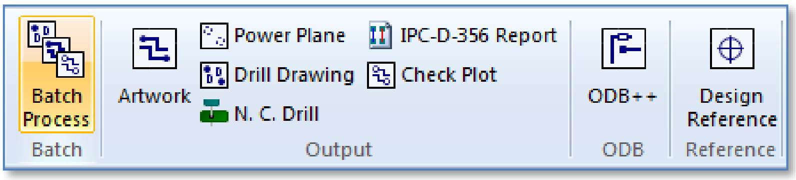



| Net | Type | Layer | X Position | Y Position | Required Number | Testpoint Number | Requirement Met | On Grid | Error | Near Pad |
|---|---|---|---|---|---|---|---|---|---|---|
| $2 | (Testpoint) | Bottom | 51.400 | 60.900 | 1 | 1 | Yes | Yes | > 0.000 | U1-2 |
| $3 | (Testpoint) | Bottom | 90.600 | 62.900 | 1 | 1 | Yes | Yes | > 0.000 | U2-20 |
| $101 | (Testpoint) | Bottom | 112.000 | 62.000 | 1 | 1 | Yes | Yes | > 0.000 | U3-20 |
| $113 | (Testpoint) | Bottom | 107.000 | 86.300 | 1 | 1 | Yes | Yes | > 0.000 | R4-2 |
| A0 | (Testpoint) | Bottom | 103.900 | 88.300 | 1 | 1 | Yes | Yes | > 0.000 | U4-A1 |
| A1 | (Testpoint) | Bottom | 104.000 | 83.600 | 1 | 1 | Yes | Yes | > 0.000 | U4-B1 |
| A2 | (Testpoint) | Bottom | 105.800 | 80.700 | 1 | 1 | Yes | Yes | > 0.000 | U4-C1 |
| A3 | (Testpoint) | Bottom | 102.700 | 80.000 | 1 | 1 | Yes | Yes | > 0.000 | U4-D1 |
| A4 | (Testpoint) | Bottom | 105.000 | 78.400 | 1 | 1 | Yes | Yes | > 0.000 | U4-D2 |
| A5 | (Testpoint) | Bottom | 104.300 | 74.100 | 1 | 1 | Yes | Yes | > 0.000 | U4-A2 |
| A6 | (Testpoint) | Bottom | 101.800 | 70.100 | 1 | 1 | Yes | Yes | > 0.000 | U4-C2 |
| A7 | (Testpoint) | Bottom | 108.100 | 83.500 | 1 | 1 | Yes | Yes | > 0.000 | U4-A3 |
| A8 | (Testpoint) | Bottom | 66.200 | 61.200 | 1 | 1 | Yes | Yes | > 0.000 | U1-39 |
| A9 | (Testpoint) | Bottom | 84.200 | 55.100 | 1 | 1 | Yes | Yes | > 0.000 | U2-18 |
| A10 | (Testpoint) | Bottom | 109.900 | 59.900 | 1 | 1 | Yes | Yes | > 0.000 | U3-17 |
| A11 | (Testpoint) | Bottom | 106.500 | 56.700 | 1 | 1 | Yes | Yes | > 0.000 | U3-16 |

Now that you have finished the design, you can select **File →Exit** from the menu bar and rebuild the results. If you didn't manage to finish the testpoint creation, just open **DesignC8_CS.pcb**, save it as **DesignC8.pcb** and then experiment to see the finished results**.**



## Step 4 - Manufacturing Data for Design C

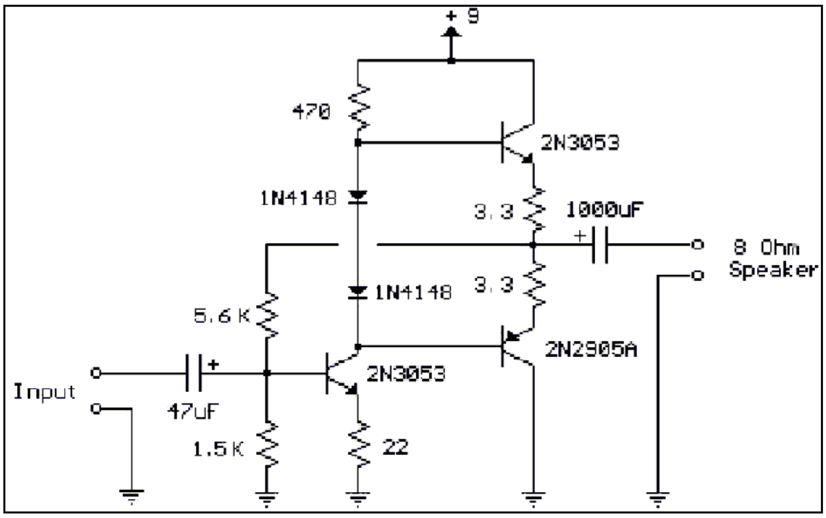



If you like, you can create the manufacturing data for this design by selecting [**Manufacture**] tab → **Batch Process**. In the Batch Process window select **[Open]**→ ***Manufacturing Output 6 Layer.ppf***, which you can find in the Self teach directory and click ***[START]***.

Check CADSTAR Place & Route Editor - Functionality Matrix on Zuken.com

Routing Matrix
Located in the Datasheets listing

# Chapter 5 - Design D (Single Sided Board Design)




Transistor Audio Amp (50 mW)

## Information on Design D - Transistor Audio Amplifier

Design D is based on the same schematics as Design B (a little audio amplifier). But this time you will create a SINGLE SIDED board and you will learn how to add jumpers on the fly. Typically, a jumper is used to bridge across other routes, the jumpers discussed here are *non-functional* jumpers and do not appear in the schematics. The sequence is the same as before.

## Step 1 - Design D

1. Open **DesignD_CS.scm** and save it as **DesignD.scm** and transfer the schematic to PCB using the **Transfer to PCB** process. Choose '***1 layer 1.6mm.pcb***' as PCB technology instead. This is a default technology file that has already been prepared for you. Notice that, although you are using the same library, the solder-pads are larger and that thicker track-widths and more spacing has been defined.

## Step 2 - PCB Placement for Design D

You can now start to place and arrange the components on the PCB after the transfer. When creating a single board design a good placement is highly important to avoid crosses in the connections, so take your time. Don't worry as you will be able in Place & Route Editor XR to add jumpers on the fly, just like adding a via.

1. Check and/or change the Units & Grid (25 thou is preferred)

2. Change the default shape type to Board

3. Draw a board outline (size 2000x1500 thou).

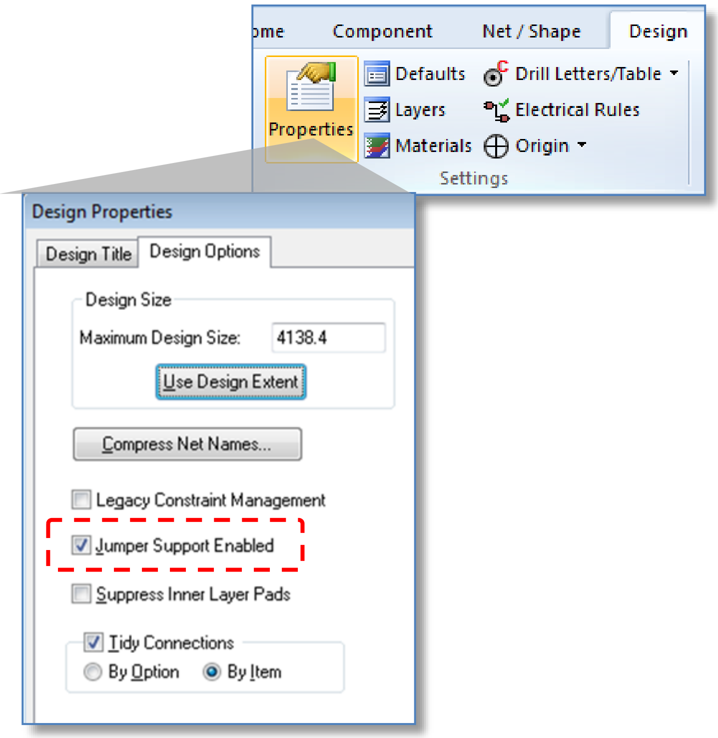
4. Arrange components around the Board Outline (Watch How in the next step)

5. Manually place and fix the critical components inside the board outline using the non-modal Item Properties panel. Cross-probe can be used if necessary.

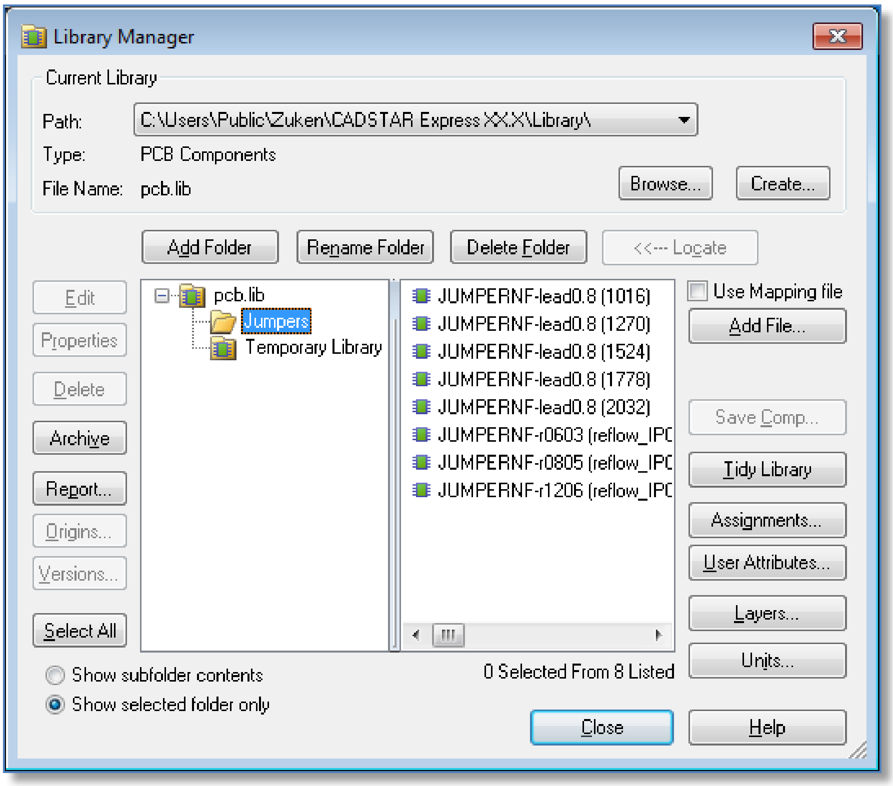
   Place VCC9V at X-position 150,0 and Y-position to 150,0
   Place INPUTGND at X-position 150,0 and Y-position to 1050,0
   Place INPUT at X-position 150,0 and Y-position to 1350,0
   Place SPK at X-position 1850,0 and Y-position to 1350,0
   Place SPKGND at X-position 1850,0 and Y-position to 1050,0

6. Automatically place the other components. If you didn't manage to place the components, just open **DesignD2_CS.pcb** and save it as **DesignD2.pcb**

7. Before going to the routing environment select the **Properties** dialog from the [**Design**] tab and ensure Jumper support is enabled on the [**Design Options**] tab.



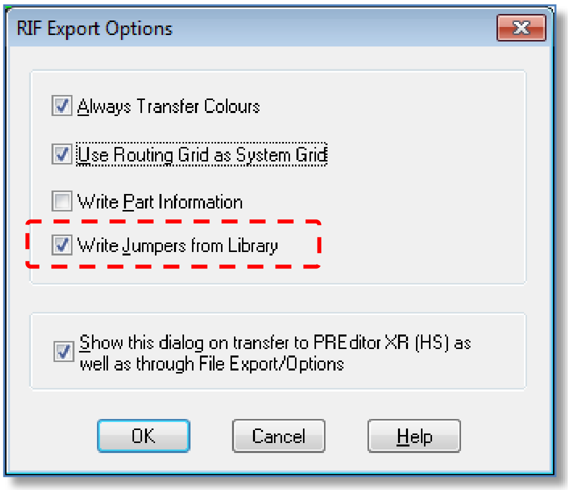
8. Also before going to the routing environment check out **Library→PCB Components**. If you expand the contents of the PCB.LIB (as shown below) you will see a sub folder for Jumpers. There are already some pre-defined jumpers, which you will be able to select in Place & Route Editor XR on the fly.



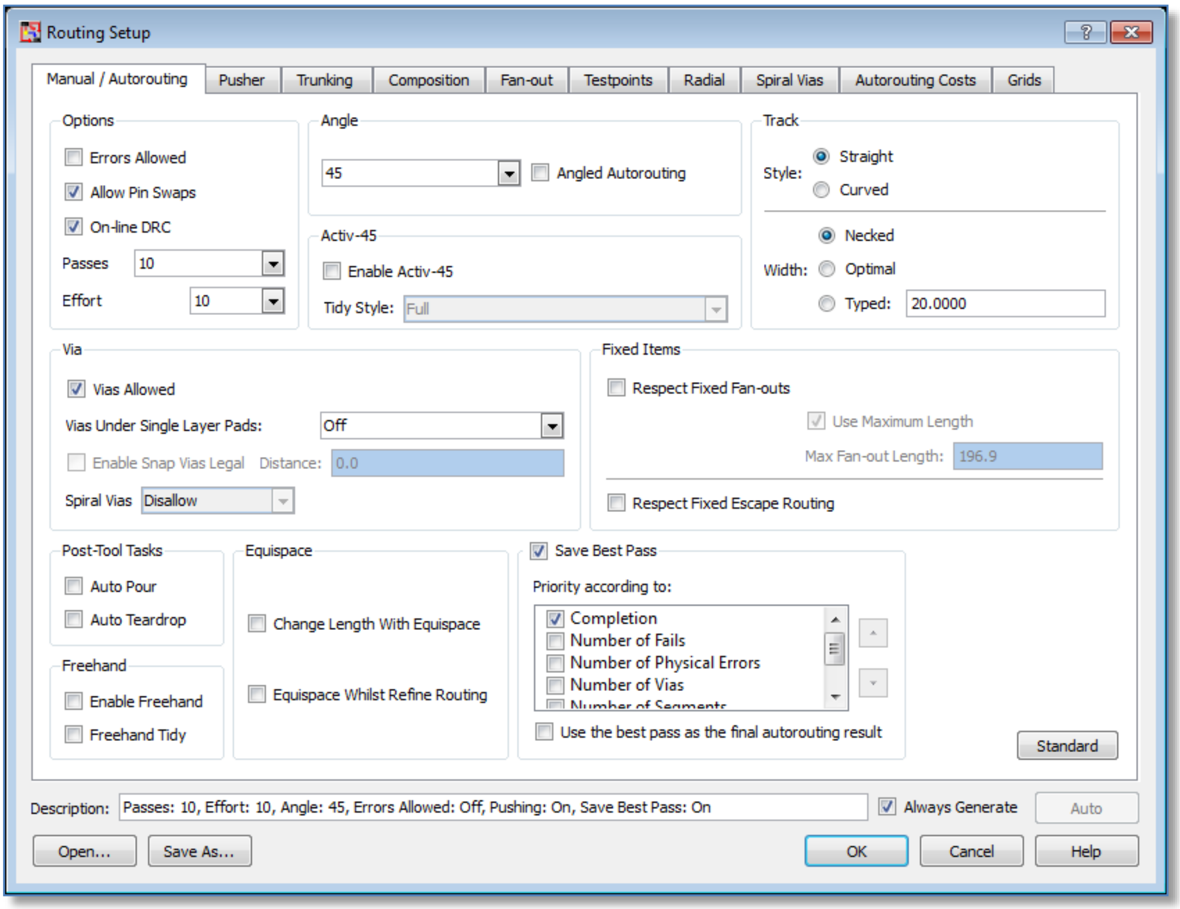

9. Open the Place & Route Editor XR2000 by selecting **Tools→PREditor XR.**

## Step 3 - PCB Routing for Design D

When transferring to the Standalone Place & Route Editor XR a *RIF Export Option* window will be showed automatically. Ensure that *Write Jumpers from Library* is ***enabled***.



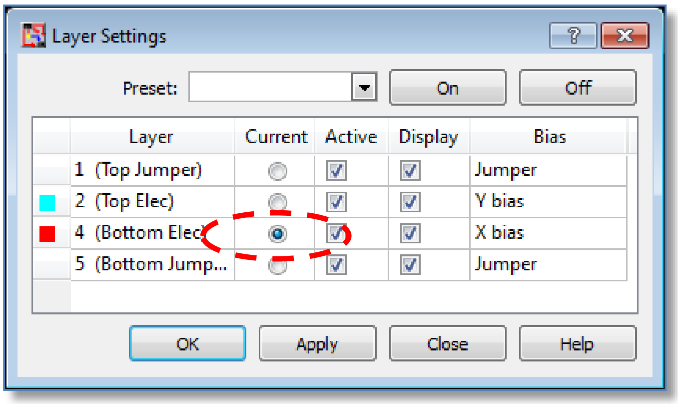

1. Before starting any routing, check the **Routing Setup** options. Select **Configure →Routing Setup [Manual/Autorouting]** tab in the menu bar (or use CTRL-T). Ensure the settings are equal to the example. If you don't like copper to be poured automatically disable it. If you don't like routes to be pushed you can disable the *Pusher* or reduce the *Effort* in which case less routes will be pushed aside.



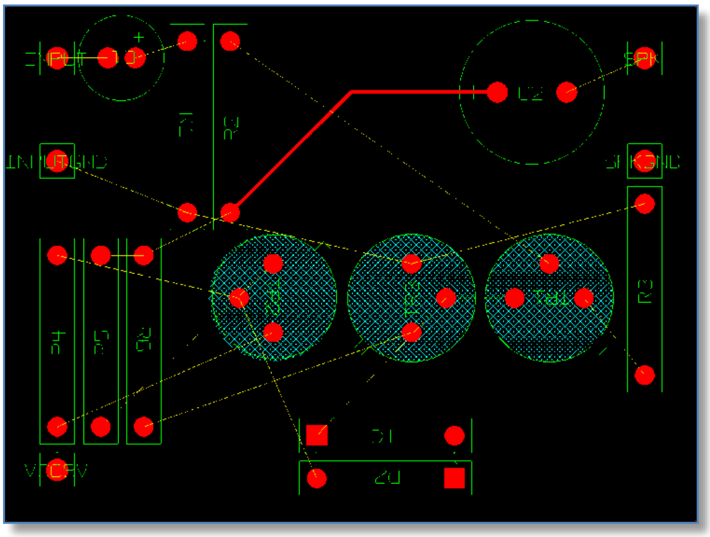
2. Click the **[Layer** {current layer}**]** selection on the menu bar. Change the Current Layer to **Bottom Elec** as shown to the right →

   Click **[OK]**.

   **Note:** 2 layers have been added to this technology (Top Jumper and Bottom Jumper)!

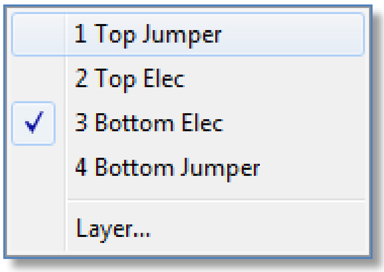


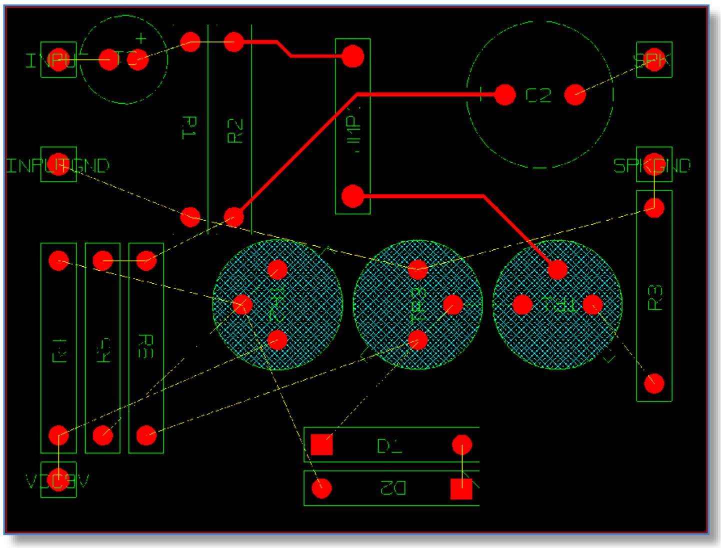

3. Manually route the net using the ***Item*** focus mode between resistor R2 and capacitor C2 as in the example on the Bottom Elec layer.



In the next step you will add a jumper *on the fly* by manually routing  the net between transistor TR1 and resistor R2 as shown in the example below on the Bottom Elec layer.

4. Route to the location you want to add the first pad of the jumper and double click, select *Top Jumper.* Now move the cursor to the location you want to add the second pad of the jumper. P.R.Editor XR will show you a thin line representing the pitch of the pre-defined jumpers depending on the available space. Double click again and you will add the jumper and you can continue routing. P.R.Editor XR will show you only a list of pre-defined jumpers if more than one jumpers with the same pitch have been defined in the library. It's as easy as adding a via!

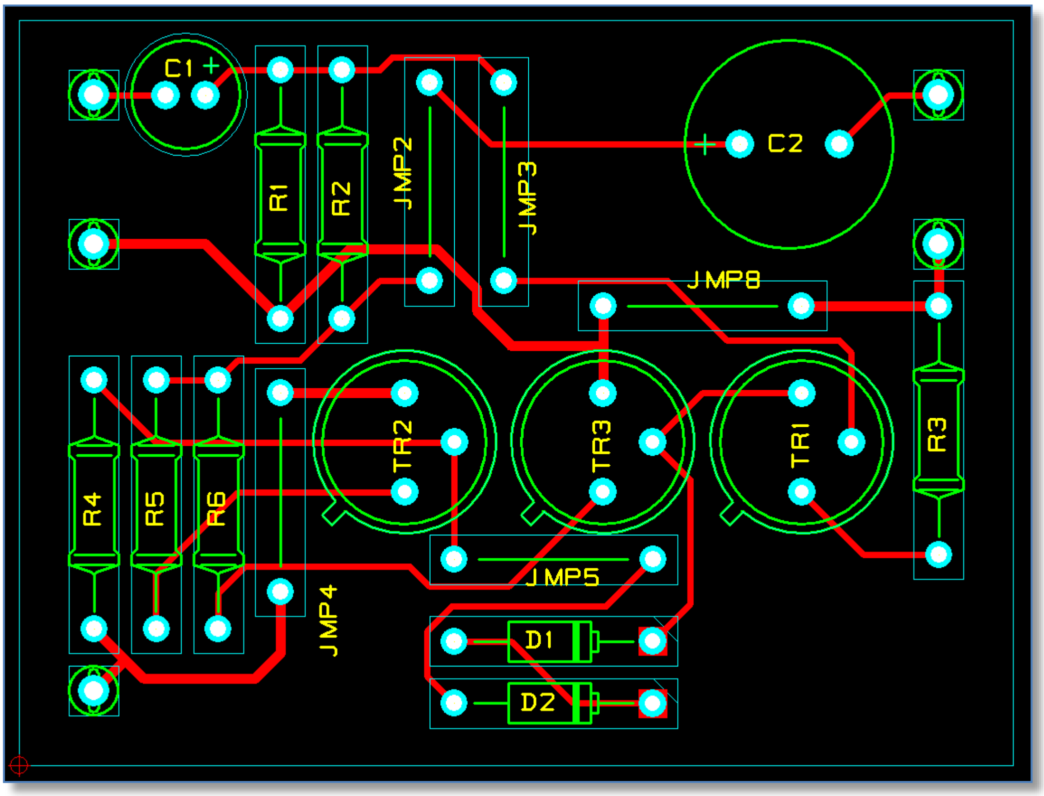


5. Now route all the connections on Bottom Elec layer and insert jumpers if necessarily.

6. Once you have finished the design you can select **File→Exit**. All routing and jumpers will be back annotated to the PCB Design. Running an ECO update won't remove jumpers and the jumpers will appear normally in the Part List and placement data.

If you didn't manage to complete the design, just open **DesignD3_CS.pcb,** save it as **DesignD3.pcb** and then experiment to have a look.




DesignD3 after Placement & Routing – your routing may be different.

## Step 4 - Manufacturing Data for Design D

At this stage, you can also create the manufacturing data (Gerber, N.C.Drill, Parts List, Placement data etc.) for the manufacturing of the PCB (as you did for Design A) by selecting [**Manufacture**]tab→ **Batch Process**. In the Batch Process window you select [**Open**] and use ***Manufacturing Output 2 Layer.ppf*,** which you can find in the User directory and click [**START**].

| | Use | Description | Process Type |
|---|---|---|---|
| 1 | ✓ | Gerber Copper pattern Componentside | Artwor |
| 2 | ✓ | Gerber Copper pattern GND layer | Power |
| 3 | ✓ | Gerber Copper pattern Inner 3 | Artwor |
| 4 | ✓ | Gerber Copper pattern Inner 4 | Artwor |
| 5 | ✓ | Gerber Copper pattern VCC layer | Power |
| 6 | ✓ | Gerber Copper pattern Solderside | Artwor |
| 7 | ✓ | Gerber Solderresist Componentside | Artwor |
| 8 | ✓ | Gerber Solderresist Solderside | Artwor |
| 9 | ✓ | Gerber Silkscreen Componentside | Artwor |
| 10 | ✓ | Gerber Solderpaste Componentside | Artwor |
| 11 | ✓ | PDF Assembly Componentside | Artwor |
| 12 | | [illegible]rtlisting | Report |
| 13 | ✓ | [illegible]mentdata | Report |
| 14 | ✓ | Drillda[illegible]ted Through Holes) | N.C. Dril |
| 15 | ✓ | Drilldata (Non-Plated Through Holes) | N.C. Dril |
| 16 | ✓ | Layer Stack-up report | Report |

You can easily *disable* the rows that you do not wish to post-process. In this design, since it is a *single layer board*, the layers that are to be generated are *Bottom Elec, Top Solder Mask, Bottom Solder Mask and Top Silkscreen* (all in Extended Gerber RS274-X format). Other additional manufacturing data that CADSTAR can generate which is necessary for manufacturing are *Parts Lists, Placement Data and Drill Data*. All manufacturing data will be saved in the *Output* directory.

Alternatively you might want to produce an **ODB++** output file. ODB++ is one of the most intelligent CAD/CAM data exchange formats available today, capturing all CAD/EDA, assembly and PCB fabrication knowledge in one single, unified database.

# Conclusion

After these five exercises you should now be more familiar with the basics of PCB design. In the near future you may even be designing a more complex PCB using CADSTAR.

With this booklet, you have received a free copy of CADSTAR Express. CADSTAR Express provides a number of features of the full CADSTAR version, only limited by the number of components (max 50) and pads (max 300).

For further information on pricing or if you require any support during evaluation or prefer to receive a detailed demonstration, please contact your local CADSTAR distributor:

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There are also other CADSTAR tools that help Schematic and PCB designers to create board layouts.

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