ZUKEN®

CR-8000™

Graphical Pin Manager
FPGA/PCB Co-Design

Top Benefits and Features

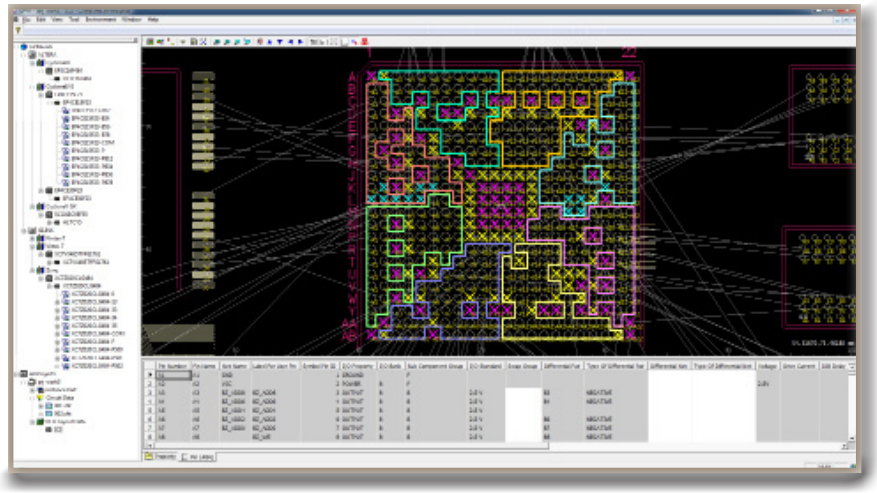
- Concurrent design flow for FPGAs and PCBs, from library creation to physical design.
- Up-to-date support for Xilinx, Altera, Lattice and Microsemi device kits, including I/O constraints for accurate part development.
- Accurate control and traceability of critical details for programmable devices using Project Management system.
- Reduce part creation time with automatic creation and splitting of logic symbols and direct integration with Component Manager.
- Reduce design iterations with direct exchange of pin constraint and report files from Altera Quartus II, Xilinx ISE/Vivado, Microsemi Libero, Lattice ispLever/ Diamond and Aldec Active-HDL.
- Automatic creation, editing and checking to reduce effort in design output.
- Support for BSDL, CSV, VHDL/ Verilog, and existing library data for high-pin count device design.
- Optimize I/Os with interactive and automatic pin swapping.
- Generate pin swap reports to compare document changes during FPGA and PCB design.

Introduction

Engineers continue to embrace programmable logical devices within their product designs in numerous applications across a wide range of industries. With FPGAs incorporating embedded processors, memory blocks and DSP functions, they are an attractive, low-cost option for many designs.

FPGAs can now replace ASICs in many design applications. They are also used for prototyping designs, implementing ASICs, or other embedded hardware and software design as they can easily be reprogrammed. However, rising device complexity means high pin counts, which bring about new challenges and higher costs when integrating these devices into the PCB. Engineering teams require an effective design flow, unifying FPGA and PCB design to reduce design cycle times and improve time-to-market.

Zuken's Graphical Pin Manager (GPM) offers an effective FPGA/PCB co-design environment, providing support for the latest devices offered by FPGA vendors such as Xilinx, Altera, Lattice, and Microsemi. As part of Zuken's CR-8000 system-level design suite, GPM enables design teams to intelligently communicate pin I/O assignment information on FPGAs or other high pin count devices with Design Gateway, Design Force and other FPGA vendor tools. This allows programmable devices to be developed in parallel with the PCB design and means these devices are ready to meet project delivery schedules and are available for production. GPM is also compatible with CR-5000 System Designer and Board Designer.

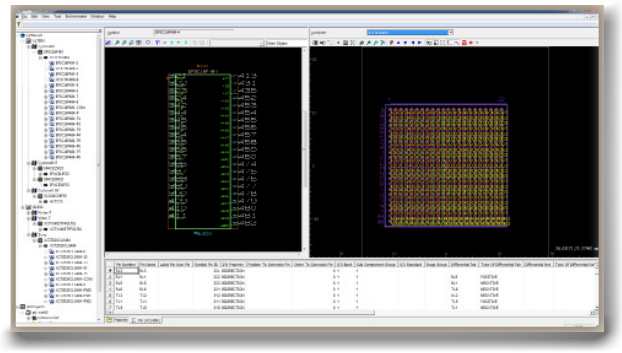


Enable FPGA/PCB co-design with Graphical Pin Manager

Device Selection and Library Creation

FPGA designers and librarians can import pin assignment information directly from FPGA design suites like Altera Quartus II, Xilinx ISE/Vivado, Microsemi Libero, Lattice ispLEVER/Diamond and Aldec Active-HDL, or use BSDL, VHDL/Verilog, or CSV files. GPM also offers an extensive library of FPGA vendor device kits for Altera, Xilinx, Microsemi and Lattice, providing additional key attributes for I/Os such as differential pairs, pin type, I/O bank and power/ground assignments. Zuken offers up-to-date downloads of design kits from our website to access the latest devices from FPGA vendors.

Once the part information is loaded into GPM, users can access easy-to-use wizards to automatically generate split symbols for immediate use in logical circuit design. GPM is also integrated with Component Manager, so users can access the library to associate required physical footprints, and export symbols and other part information directly to the library for fast part creation. Once the pin assignment is defined in GPM, the pin constraints file can be exported to the FPGA design tools.



Automatic creation and splitting of symbols and library integration eases part creation

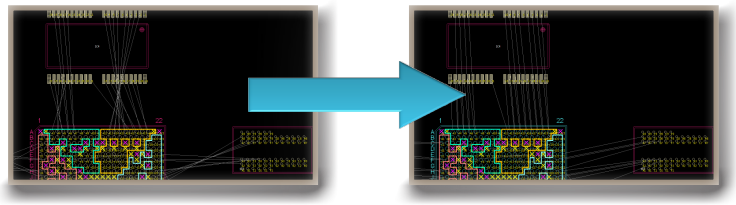
Project Management

To enable a co-design process for managing the design of FPGAs, ASICs and other high-pin count devices, GPM provides a complete project management system for these devices on the PCB. GPM allows users to load and view the logical and physical design for the PCB, along with the device instance in the project and the library. This allows users to control and communicate changes directly to all stages of the product design process.

I/O Optimization and Pin Swapping

As the initial FPGA is being simulated and synthesized, engineers can load the logical and physical circuit design within GPM. Engineers can review the current pin assignment and each of the constraints and rules associated to each I/O, and use the extensive set of utilities to visualize the FPGA on the PCB. The FPGA can be viewed with colored I/O banks, or as the sub-element model defined when splitting the component. This simplifies analysis of how the FPGA is structured and how the interconnect relates to other components on the board.

GPM also provides a ratsnest view of the board, showing the connection between pins or from partially routed signals. For rules-driven optimization of the I/Os, the user can interactively conduct pin swaps with visual indicators highlighting the candidates allowed for swapping with the selected net. Users can also use the automatic pin assignment optimization feature that will untangle the ratsnest for the selected FPGA component instances.

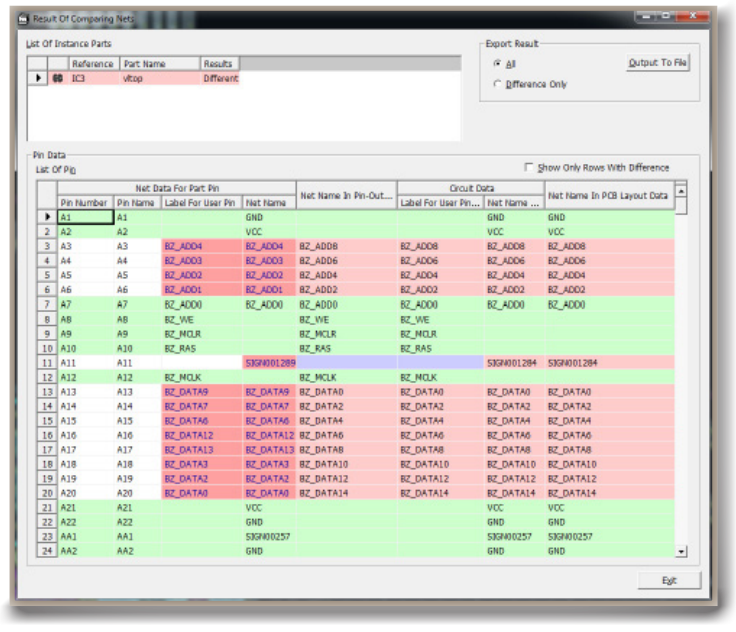


Automatic I/O optimization improves PCB routability and reduces cost

Design Synchronization

Once the pin assignment is fixed, users can instantly compare the results of the interactive or automatic pin swaps on the design. The net comparison report allows the user to select between the device instance at the library, schematic and PCB level, and export the result into a text file. This allows simplified visualization and traceability of the changes conducted on the design, and accurately communicates those results.

To synchronize each part of the design process with the updated pin assignment, GPM can export the results directly to the logical and physical circuit data, and to the library. It can also generate a vendor-specific pin report file that can be loaded into the FPGA design tools. This saves time and eliminates the error-prone process of manually communicating changes. Users can also export the pin assignment changes in HDL or CSV format.



Generate pin swap reports to compare document changes during FPGA and PCB design