ZUKEN®

CR-8000™

Chip-Package-Board Co-Design

Design Force

TOP FEATURES AND BENEFITS

- Multi-board constraint browser to view and analyze system level interconnects.
- Automatic ball assignment with the ability to optimize complex routing solutions.
- Interposers supported with through-silicon-vias (TSV) and bidirectional support for exchanging System on Chip (SoC) information using industry standard formats.
- 2.5/3D stacking structures handled in any configuration: stacked, adjacent, interposers, with wire bond and flip chip packages.
- Rule driven I/O placement Redistribution Layer (RDL) router that supports 45 degree, multi-layer, and multi-region routing.
- Rapid scriptable design and feasibility studies for die sizing; I/O placement (area and peripheral); bump planning, RDL placement, and escape routing.
- Numerous routing engines enable rapid feasibility or detailed RDL and bump escape routing of signals and power and ground nets.

Introduction

Today's advanced-node IC designs are challenging architects, designers and manufacturers to develop error-free and accurate data to produce right- the-first-time market solutions. Lower budgets and price pressures are pushing formerly separate design silos into one of two design scenarios:

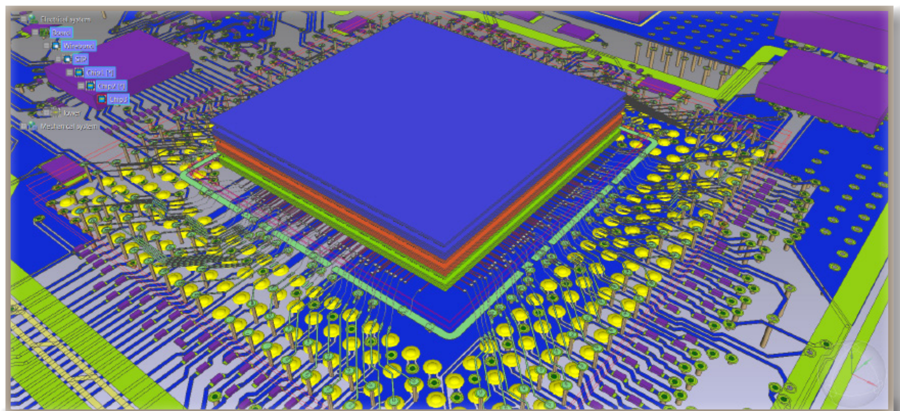
1. Multiple re-spins with second and third turn optimization putting enormous cost and time-to-market pressure on design teams.
2. Concurrent chip, package and board co-design with reliable, real-time shared design data continuously throughout the design and verification process.

Concurrent chip, package and board co-design provides lower package cost and reduces PCB cost through resultant layer reductions.

Comprehensive system co-design recognizes the interaction between chip, package, and board data to reduce complexity, size and cost of the overall system. Zuken's Design Force native 3D chip, package and board co-design enables optimization of the chip-package-board interface throughout the design flow to address these market advantages.

As the industry moves from coplanar designs to complex 3D stacked structures and embedded devices, the need exists for tools that can accurately render and provide meaningful visual and DRC feedback to enable, rapid right-the-first-time designs. Design Force's inherent chip, package and board co-design capabilities enable realtime 3D hierarchical design, allowing design teams to concurrently create any combination of advanced stack dies, packages and PCBs.

In Design Force multiple co-design configurations for chip, package and board are supported such as SoC/package, package and PCB and SoC/System in Package (SiP)/PCB co-design. Design Force chip, package and board path finding solution uses industry standard OpenAccess die database to optimize system design. Users can also automate and configure rules-based perimeter I/O and area I/O planning and placement. The solution also provides bump planning/placement and a feature-rich die and interposer Redistribution Layer (RDL) and escape router.



Chip-Package-Board co-design in native 3D

2.5/3D IC Design Solution

Design Force chip, package and board co-design provides a technology-rich and device-rich design environment for implementing traditional and advanced node design structures like die + package + PCB, SiP, PiP, and interposer + TSV.

Design Force is a platform that you can rely on today and can scale to tomorrow's technology challenges.

Methodology

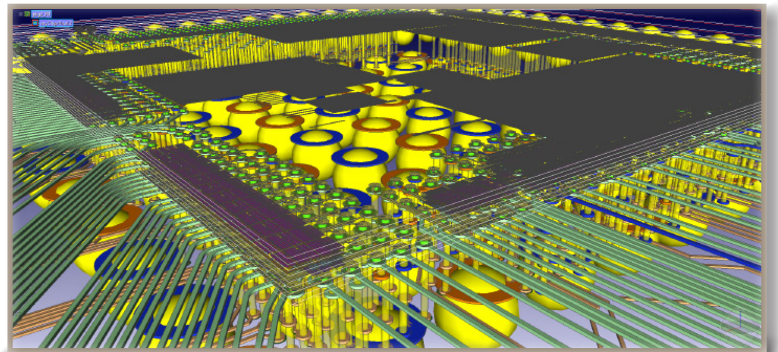
Design Force chip, package and board co-design has been developed to facilitate the innovation of high-performance electronic solutions, whether for consumer electronics, automotive, industrial, medical or mil/aero. To meet the challenges of Moore's Law induced technology requirements, system architects and designers require exotic non-planar structures like SiP, Package on Package (PoP) and Package in Package (PiP). Advantages such as increased density, lower power and more reliable signaling can only be achieved with accurate tool feedback. Design Force Chip-Package-Board Co-Design provides a visually rich concurrent 2D/3D design environment to aid designers in transitioning toward these structures. As a unified IC, packaging and PCB solution, Design Force Chip-Package-Board Co-Design provides a single environment solution for maximum system optimization.

Interface to best-in-class CAE tools

Design Force supports integrations to best-in-class tools from partners such as ANSYS, AWR, Agilent and Synopsys for RF, Full Wave FD/TD, power integrity, and thermal extraction and analysis. This allows designers to address key issues early in the design process. Design Force also contains native EMI, signal and power integrity analysis for eliminating design errors.

Additional features of co-design

- Silicon interposer autorouting and optimization of TSV layout further improves the quality of 2.5D/3D IC design and reduces design cycle times
- RDL and bump templates promote IP reuse, rapid prototyping and design tradeoff studies
- IC co-design structures imported with Library Exchange Format / Design Exchange Format (LEF/DEF) are easily placed and manipulated using intuitive and well documented scripting environments using industry standard Tcl programming language
- User configurable menu buttons and menu bar enable a highly customizable UI allowing reuse for executing common functions and routines
- Automate design tradeoff studies, such as:
    - RDL and die escape routing studies
    - Die size, perimeter I/O, and area I/O placement studies
    - Bump pitch and signal-power-ground ratio studies
- Support for non-uniform bump pitches, bump pitches by interface, geography, or power grouping
- Die escape router promotes rapid go/no go answer for bump studies
- Package feasibility router predicts likelihood of routing success for multi-layer package designs at the bump/ball pattern definition stage.



Flip chip with redistribution layers in native 3D

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