ZUKEN®



*Complete PCB design environment – from initial concept through to product realization.* 



**TEWS** significantly reduces development time and cost of complex high-speed PCBs using concurrent power integrity simulation



"We are now creating more right-the-firsttime designs and one of the biggest benefits is being able to reduce the number of decoupling capacitors, which adds up to a significant reduction in manufacturing costs."

Michael Költzow, Senior CAD Engineer, TEWS Technologies, Hamburg-Halstenbek, Germany



TEWS significantly reduces development time and cost of complex high-speed PCBs using concurrent power integrity simulation

TEWS Technologies encountered challenges around power distribution on PCBs for their embedded interface modules, due to today's increasingly complex designs. By adding CADSTAR Power Integrity Advance module to their high-speed design flow they are now meeting targets for right-the-first-time designs and achieve rapid compliance with power integrity constraints.

Like many companies working with FPGAbased boards, TEWS Technologies faces increasing power integrity challenges due to the multiple voltage rails needed by the ICs they use. Today's designs can contain dozens of power distribution networks (PDNs), creating complex design scenarios for the engineers who have to make them work. In addition, they needed to meet the highly complex impedance targets and decoupling requirements specified by their semiconductor vendors, while still complying with signal integrity rules.

TEWS had been using Zuken's CADSTAR solution for its PCB design process for more than 15 years. Motivated by the advanced solutions and continuous innovation of the CADSTAR flow, they increased their use of different high-speed options in recent years. Making full use of tools such as advanced high-speed modules for constraint management and constraint-driven routing and signal integrity simulation in pre- and post-layout phases has allowed them to deliver leading-edge technology to their customers.

Following a benchmarking study, TEWS recently made the decision to add the CADSTAR Power-Integrity Advance module to their sophisticated highspeed design flow to address design problems around power distribution on their PCBs.

### Addressing power integrity issues early in the design phase

Ralf Brüning, Senior Product Specialist for high-speed and analysis tools at Zuken EMC Technology Center Paderborn, Germany, worked alongside TEWS in the initial implementation to ensure smooth setup of the new analysis module. Several initial projects were designed to shorten the tool introduction phase, and Brüning made sure there was close cooperation in the initial stages.

"We had been working with TEWS on their sophisticated designs in several projects for a number of years, which made getting the project up and running much easier. Having an established high-speed process in place also made it more straightforward when it came to enhancing the design process analysis capability, as information such as IBIS models was already available for each new design," says Brüning.



Current density result for detecting potential hot-spots

#### **Results**

- Power integrity simulation helped create right-the-first-time designs and ensure rapid compliance with power integrity constraints.
- Achieved goal of designing a power distribution network capable of providing charge to all ICs on a minimal number of PCB layers
- Reduced manufacturing costs significantly by reducing the number of decoupling capacitors.



TEWS Technologies is a privately held company based near Hamburg, Germany, with more than 30 years of experience designing and building turnkey, embedded interface solutions. Their industry-leading family of embedded interface modules is based on leading architectures such as IndustryPack, PMC, XMC, cPCI, PCI, PCIe, VME, AMC and FMC – addressing the requirements of communications and networking, analog, digital, field-bus, motion control applications and programmable FPGA solutions.



A complete design environment for PCB design – from initial concept through to product realization.

## ZUKEN®

# CADSTAR

CADSTAR is a complete design environment for PCB design – from initial concept through to product realization.

With a unified suite of applications, engineers can seamlessly define, visualize, implement and verify their designs. Optimized for the typical small and mid-sized design team, it also appeals to individual all-rounders and corporations operating across multiple sites.

"Zuken's Power Integrity Advance allows us to extract extremely accurate information on the power integrity behavior, decoupling efficiency and potential IR-drop, and current density hot-spots of critical power distribution networks early in our CAD design process. This helps us to create right-the-first-time designs and ensures rapid compliance with power integrity constraints."

Michael Költzow, Senior CAD Engineer, TEWS Technologies

### Highly accurate concurrent simulation approach

Due to its high internal quality standards, TEWS was eager to verify the accuracy of the Zuken approach from the outset. For signal integrity they compared the simulation and impedance results with measurements performed by their board manufacturers. Then they compared the Power Integrity Advance analysis results with analytical attempts on specially designed structures. TEWS was pleased by the match between the simulation results and measurements and gained confidence in the power integrity simulation capabilities as well.

"It is essential for us that correct signal routing and bus termination is guaranteed to ensure reliable operation. We also need to ensure that under our extremely high quality standards, with impedance-controlled layer stack-ups and an impedance target of 55 Ohms, analysis results closely match PCB specifications for SI and Power Distribution Systems," says Michael Költzow, Senior CAD Engineer, TEWS.

#### Tight integration and ease-of-use

Költzow adds, "We found the Zuken SI Verify and Power Integrity Advance tools quick and easy to use from the outset."

TEWS soon began to take advantage of a recently added link from Constraint

Manager and high-speed routing into the Power Integrity Advance tool that allows the design engineer to perform power integrity analysis (AC and decoupling analysis, as well DC investigations) prior to full board routing. This supports a virtual power integrity prototyping environment in which the designer has full flexibility to test different design options without the delay and cost of creating a full prototype.

They also found a major benefit in the level of integration with Power Integrity Advance. Integrating signal integrity or power integrity tools into a CAD design environment often involves a translator that extracts the design database and creates intermediate files for the analysis. The resulting design process can be cumbersome: the engineer must export a design file, invoke the analysis software, make notes of the results, return to the design tool to make adjustments, and then repeat this process until an acceptable solution is found.

Zuken's integrated Signal Integrity and Power Integrity analysis modules offer a more streamlined alternative: the engineer invokes the simulator from the PCB CAD tool, works on selected elements, or even the entire design, makes design changes and immediately re-analyzes the results.

"This is a much higher level of integration than has previously been possible with third-



TEWS design within Zuken's CADSTAR PCB design tool with its 18-layer HDI stackup

## ZUKEN®

#### Investigation of critical Power Bus: +2,5V-GND: 500MHz



+2,5V\_GND +2,5V\_GND 6.03 2332.59 | 1000.00 | 1C39

### TEWS PI result (impedance profile Z11 of FPGA power supply and impedance distribution plot)

party analysis solutions. It lets us integrate analysis very early in the design process; a capability that is becoming increasingly critical to a design project's success," says Peter Zimmermann, Head of Hardware Design, TEWS.

With power integrity analysis linked directly to the CADSTAR constraintbased PCB design process, the design can be re-simulated during or after each layout step to ensure no problems have been introduced. At the layout stage, Költzow continues to work closely with design engineers who adhere to the decoupling and power distribution constraints and are fully conversant with CADSTAR PCB layout.

#### **EMI compliance**

TEWS soon realized that they were able to try different decoupling schemes, layer spacing and power distribution area layout schemes using "what-if" capabilities in a fast and efficient way. As TEWS supplies products to international markets, EMI and EMC compliance are also critical. This requirement was satisfied by using the EMI module within the Power Integrity Advance toolset, using algorithms developed at Missouri University of Science and Technology (formerly the University of Missouri-Rolla), to predict the worst-case emission levels of a PCB.

"Even though we did not expect to match chamber measurement with accurate

dBs, the ease-of-use and reliability of the results of Power-Integrity Advance EMI, together with its fast analysis, gave us important hints about radiation hot spots on the board well before we produced the first prototype," commented Költzow.

#### Decoupling capacitor reduction

Since integrating Power Integrity Advance in their design flow, TEWS has realized its goal of designing a PDN capable of providing charge to all the ICs on a minimal number of PCB layers. Their CAD designers are able to perform power integrity analysis during the power distribution layout and they work closely with electronics engineers to ensure in that way that sufficient power is being delivered to all ICs. Design changes may then dictate changes to PDNs and/or the placement of capacitors on the PCB.

"We were confident we had a layer stack-up that matched our PDN impedance target, an optimal power-net routing and an effective decoupling scheme – even before we manufactured our first board. Prototypes testing agreed with what we experienced using Zuken's simulation tools and reaffirmed our confidence that we had chosen the best possible signal and power integrity solutions for our design flow, from integration to ease of use and accurate results," confirms Költzow.

Költzow adds: "We are now creating more right-the-first-time designs and one of the biggest benefits is being able to reduce the number of decoupling capacitors, which adds up to a significant reduction in manufacturing costs."

TEWS is now looking forward to increasing its use of Power Integrity Advance's virtual prototyping capabilities in its next design projects.



IR-Drop/DC simulation result (DC voltage distribution of 1.8V)

#### **TEWS High Speed Design Flow**



TEWS high-speed design flow

All trademarks mentioned are the property of their respective owners. Copyright © Zuken GmbH. 161208

#### zuken.com/cadstar