TOSHIBA

Leading Innovation

Toshiba Case Study
RF Module Shrink (TransferJet™)

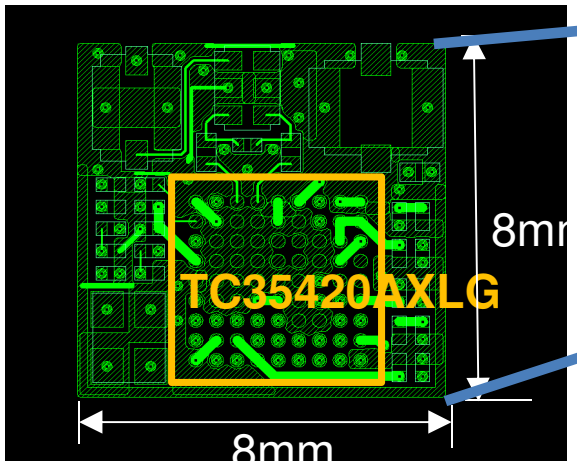
These slides are an abridgement of two presentations given by Toshiba
at the Zuken Innovation World (ZIW) conference held in Japan in 2012 and 2013.

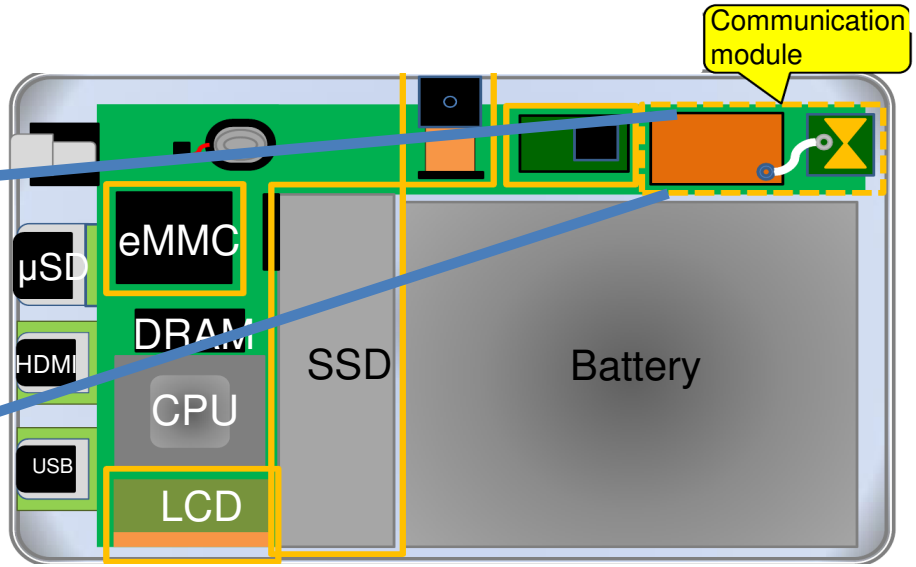
Powered by ZUKEN®

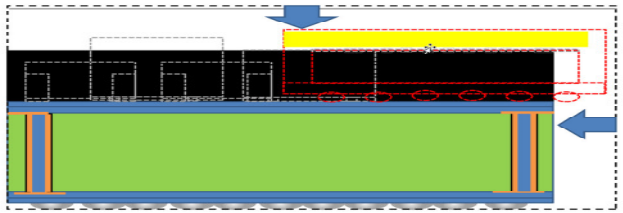
Design Force CR-8000

Project Objectives

- TransferJet™ is a standard for high-speed, close proximity wireless transfer technology.[1]
- Original design was a simple board with a wire bond package and several peripherals.
- Competitive pressures required a significant reduction in size and height of the package.
- Customer requests a module which RF matching is done to handle this technology easily.





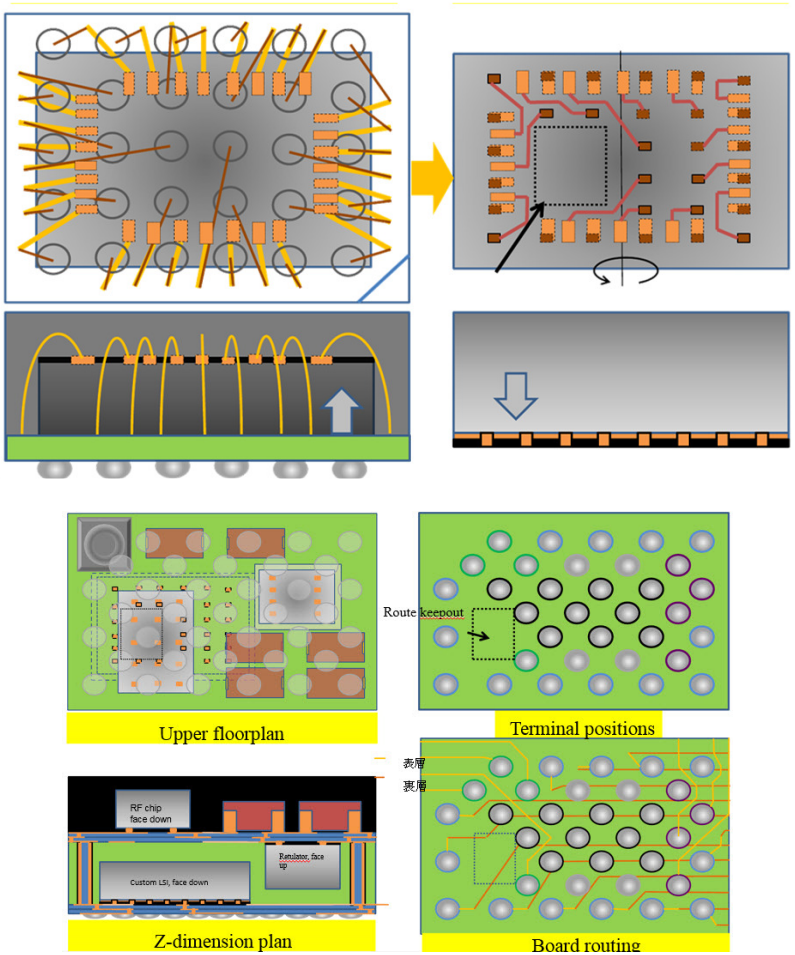


- Shrink substrate: 8mmX8mm⇒ 4.5mmX6mm
- Shrink height: 1.7mm ⇒ 1.0mm

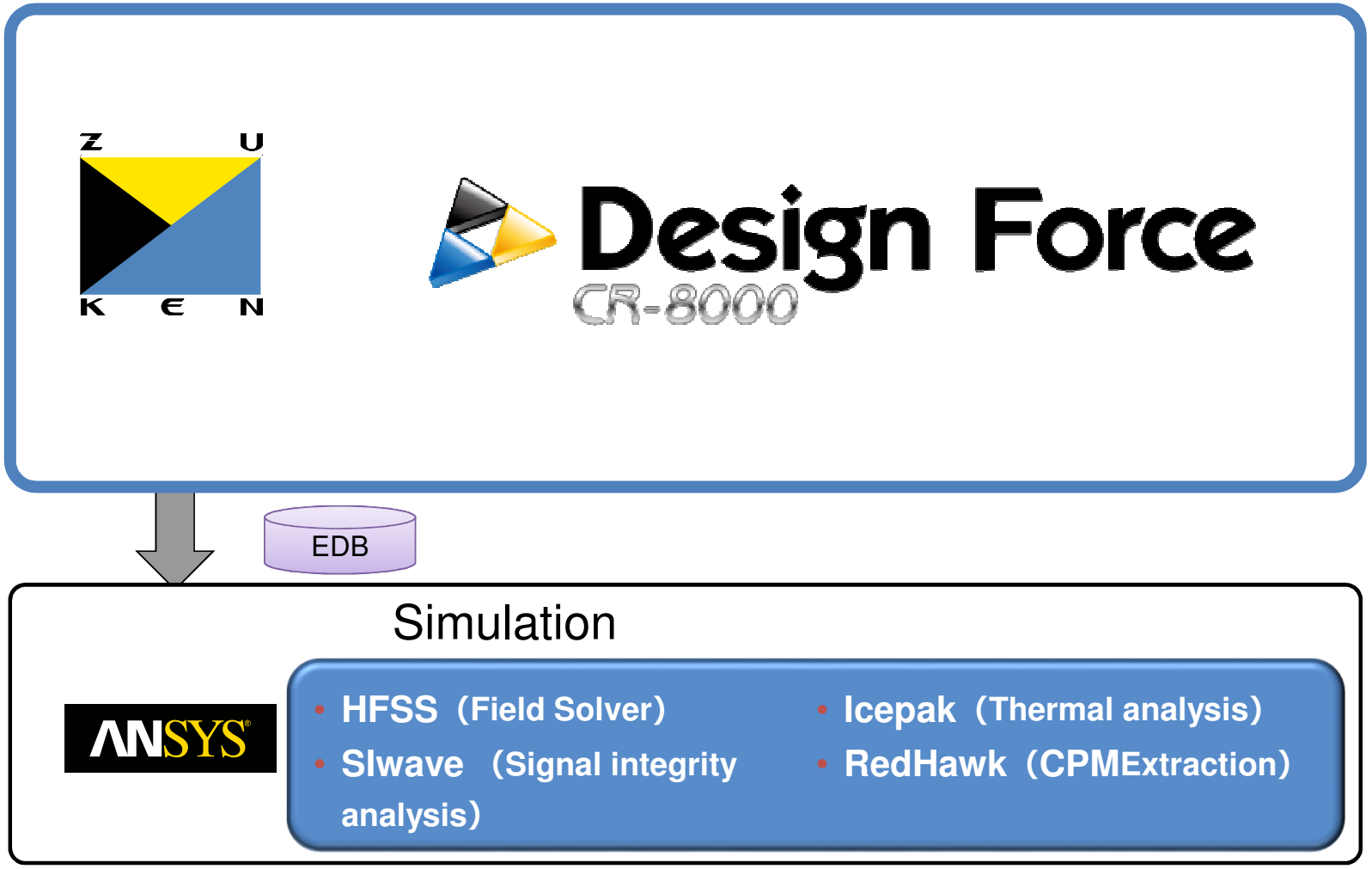
1. https://toshiba.semicon-storage.com/eu/product/wireless-communication/transferjet.html

Project Requirements

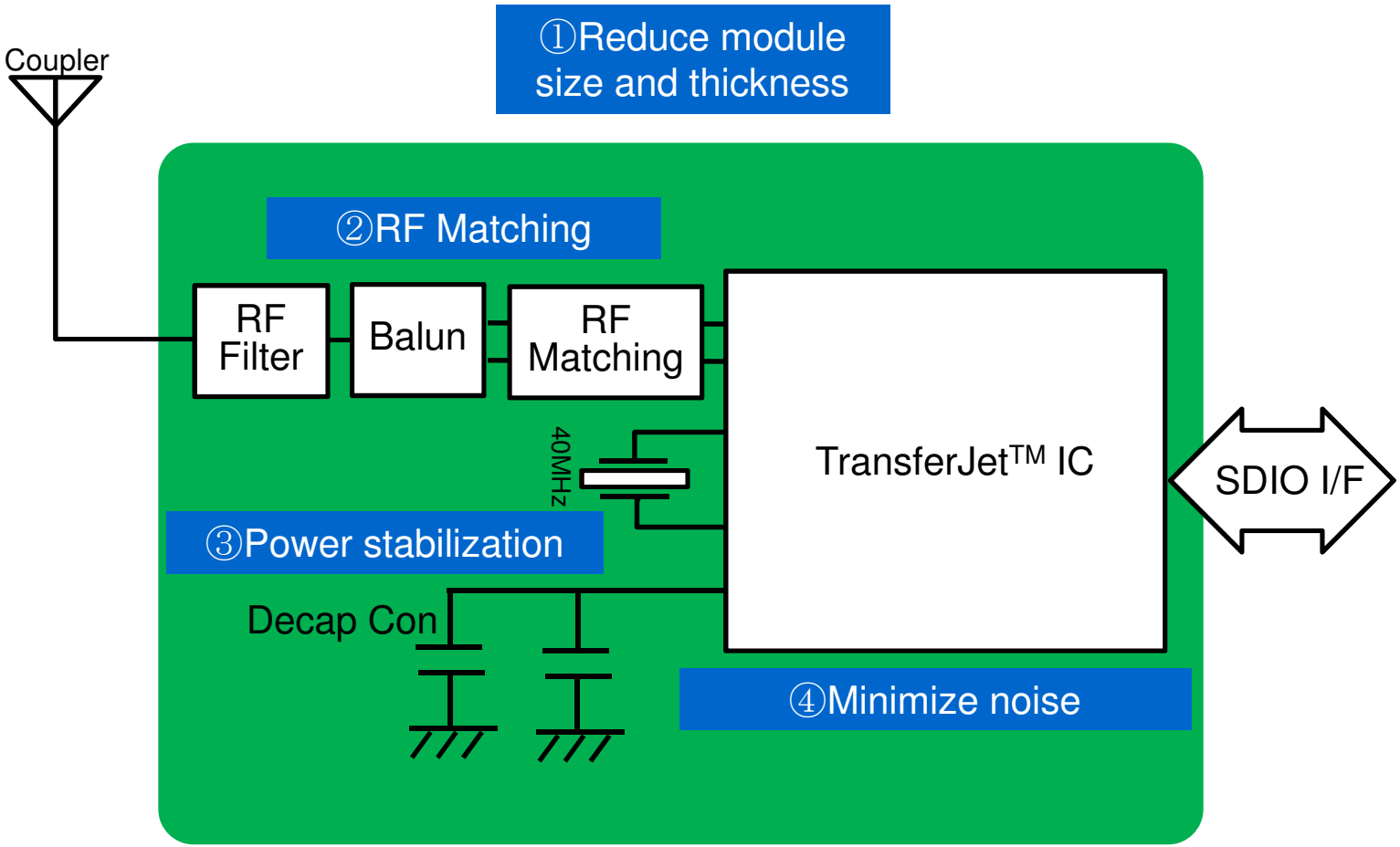
- All components could not fit on one PCB substrate
- Overall Goals:
  - Shrink size and thickness of module
  - Provide RF matching
  - Provide power stabilization
  - Minimize noise
- Decided to use bare die instead of wire bond package
- Needed to do RDL routing on the die
- Needed to embed the die
  - Added extra test pins
- Needed to co-design chip, package, board
- Needed analysis in context of system
- Needed 3D design capabilities
- Needed close collaboration with CAE tools.
- Selected Zuken's CR-8000 Design Force and Ansys analysis tools



Design and Simulation Platform

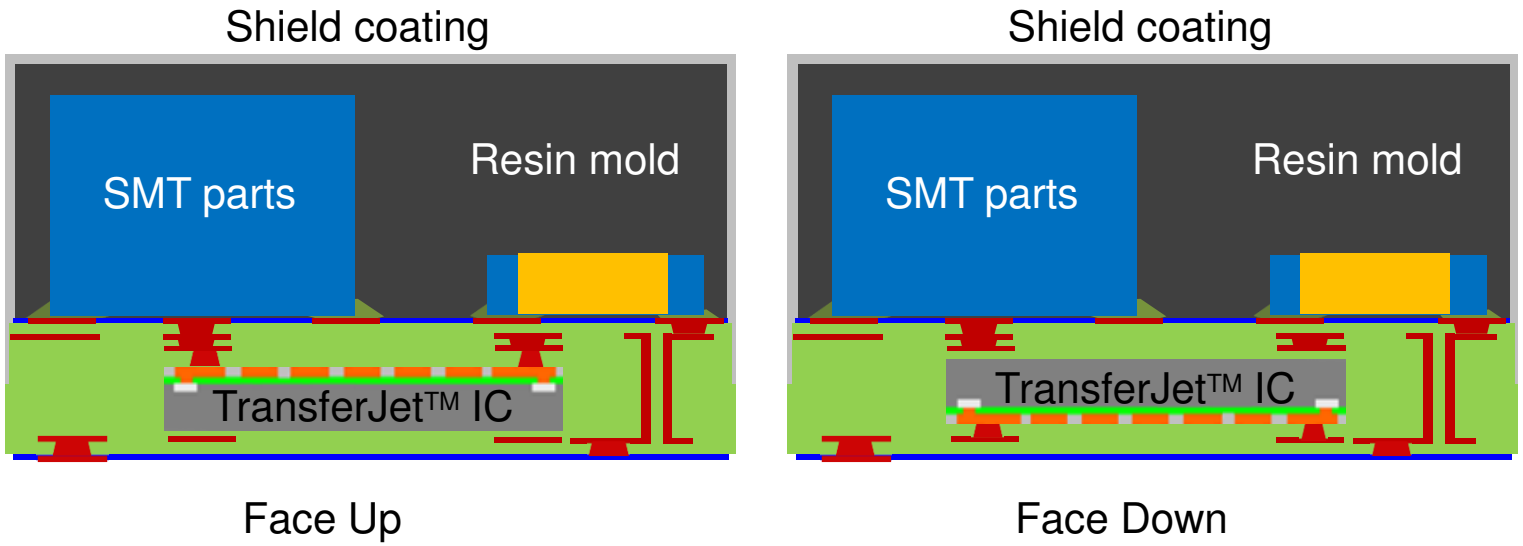


Module Block Diagram and Objectives



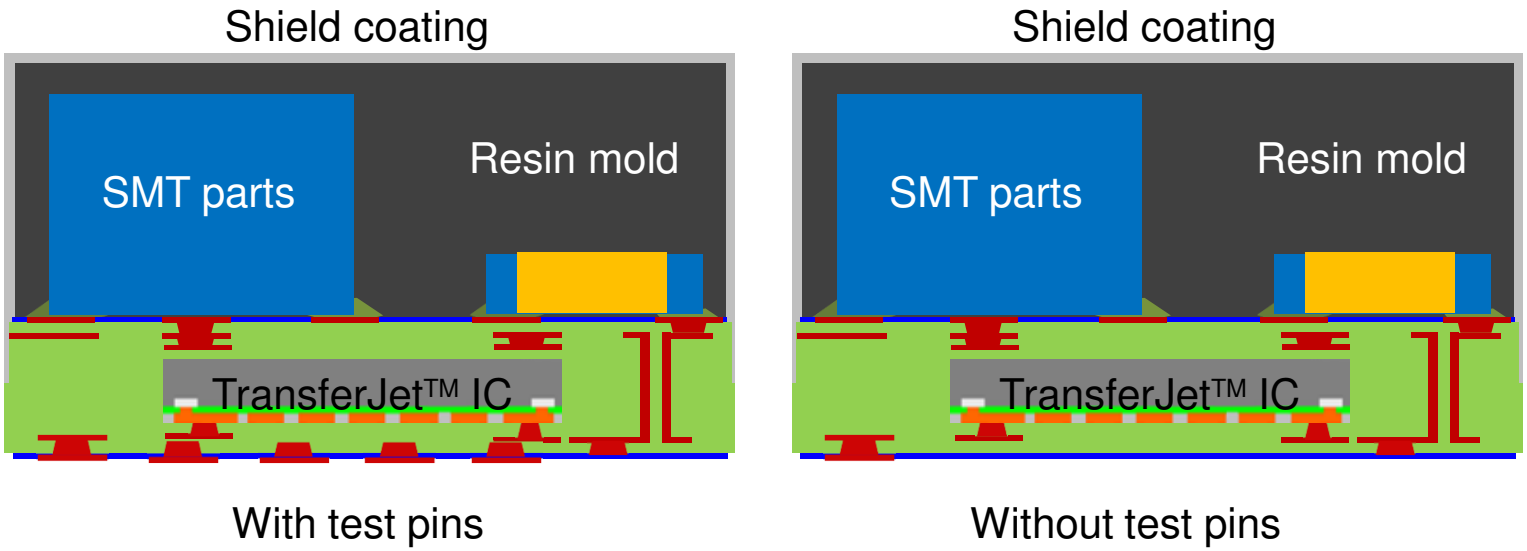
Reduce Module Size and Thickness

- Feasibility study of embedded component.
- Face Up? or Face Down?

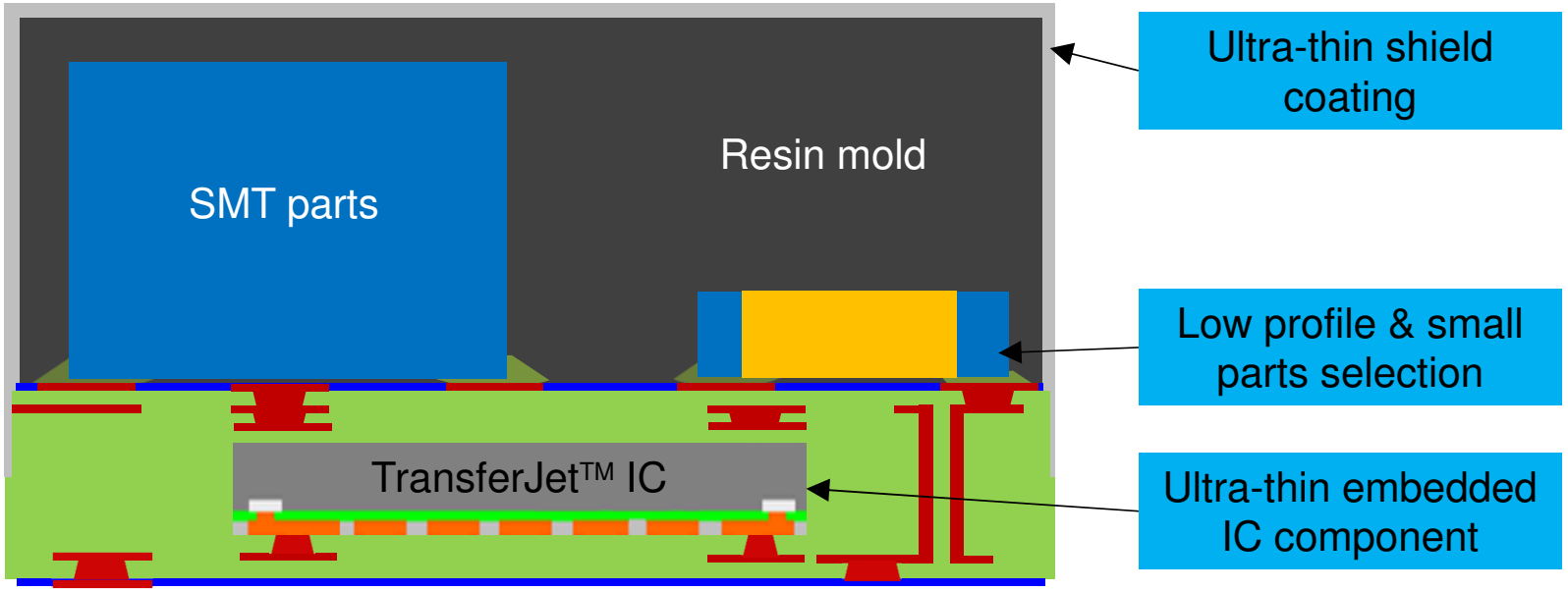


Reduce Module Size and Thickness

- Feasibility study of module pins.
- With test pins? or Without test pins?



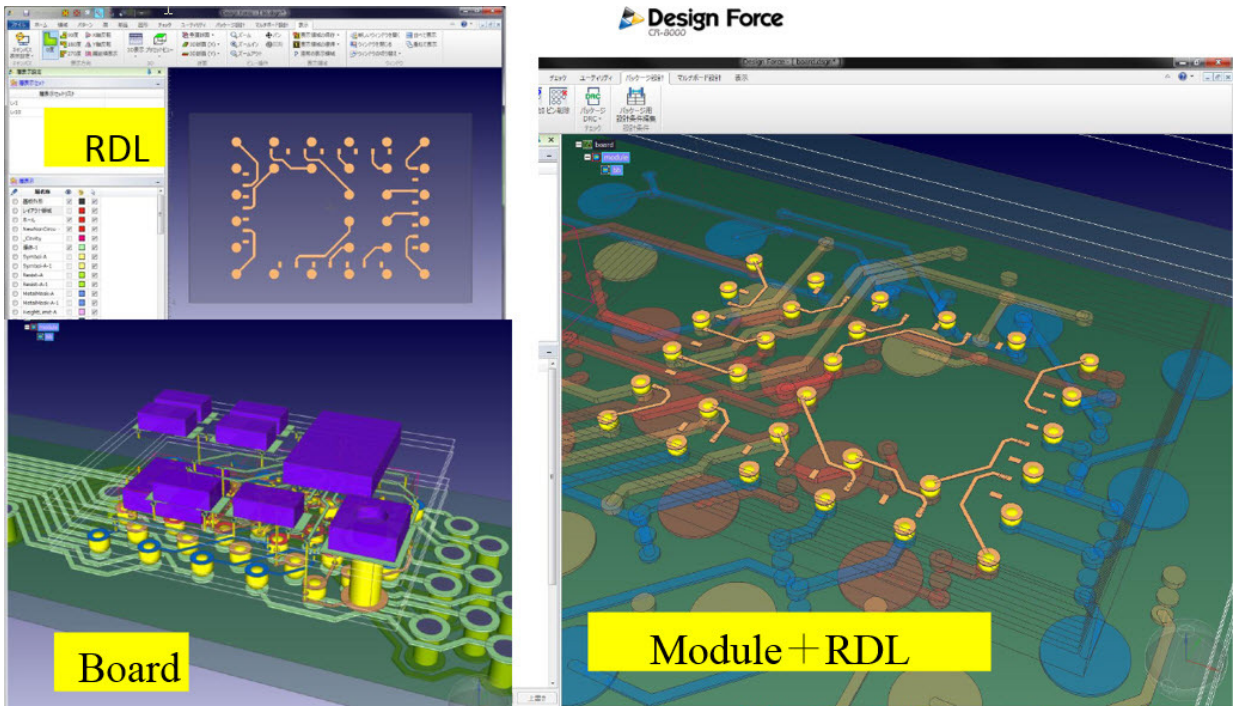
Reduce Module Size and Thickness



Reduce Module Size and Thickness

Chip-module-board Co-design in Design Force

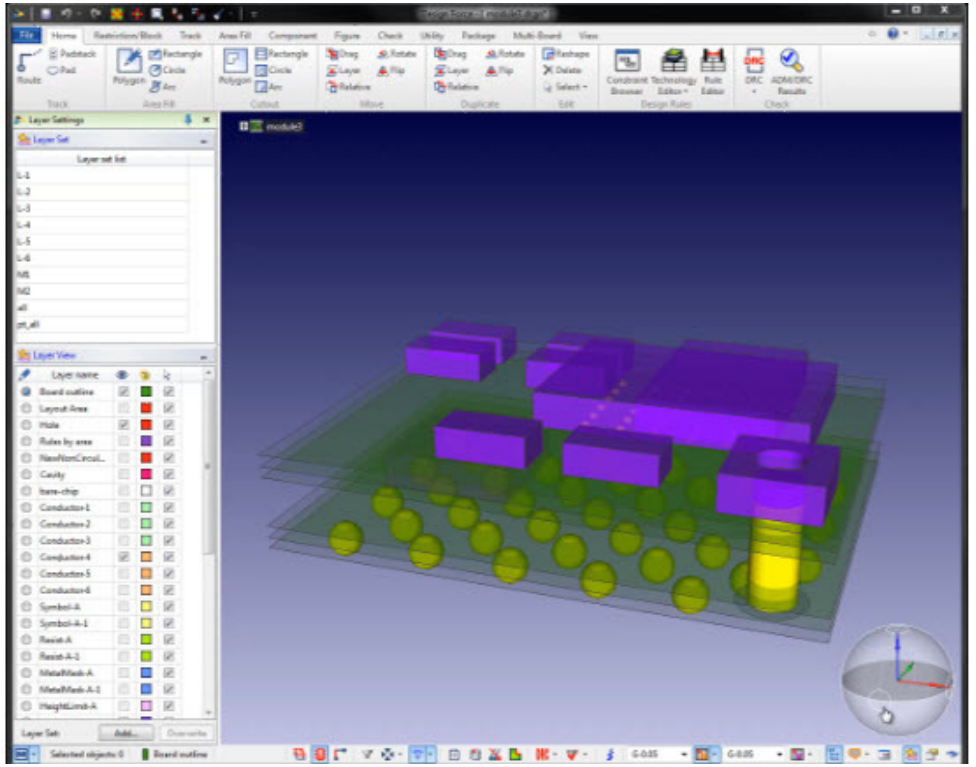
- Chip, module, and board each had different design rules.
- Easily switch context between each device to design in that device's rules
- View and design complete system in 3D or 2D on one canvas as needed



Reduce Module Size and Thickness

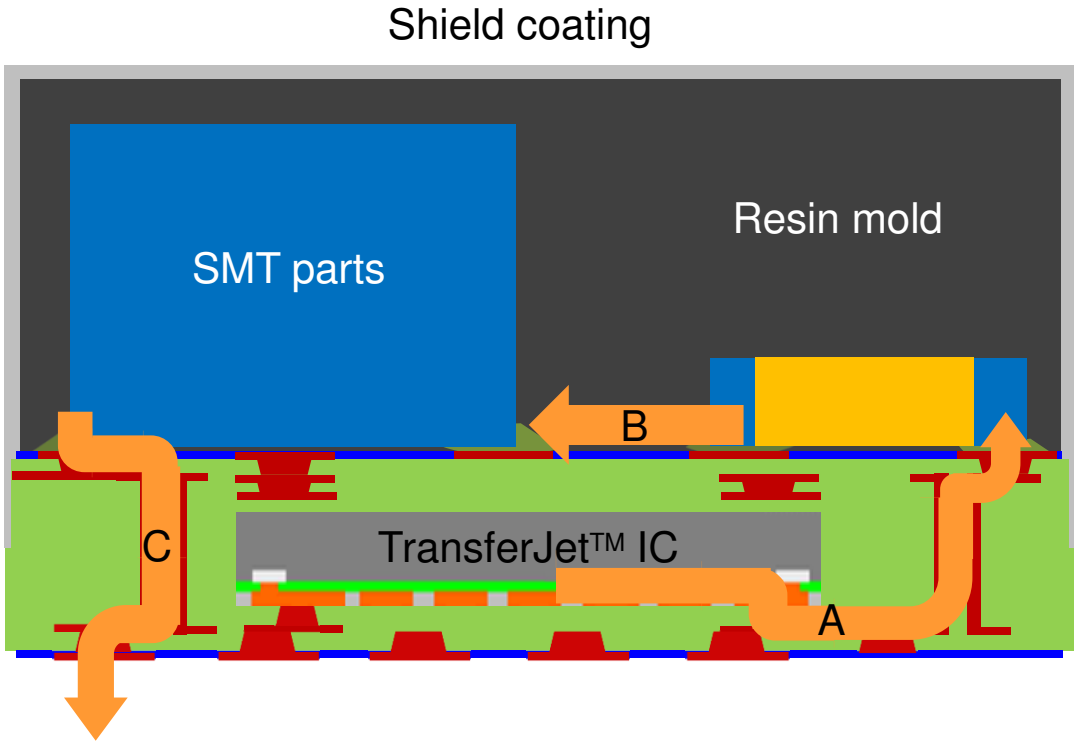
Embedding Modules using Design Force

- Embed the modules using both 2D and 3D modes
- Assign nets
- Route nets



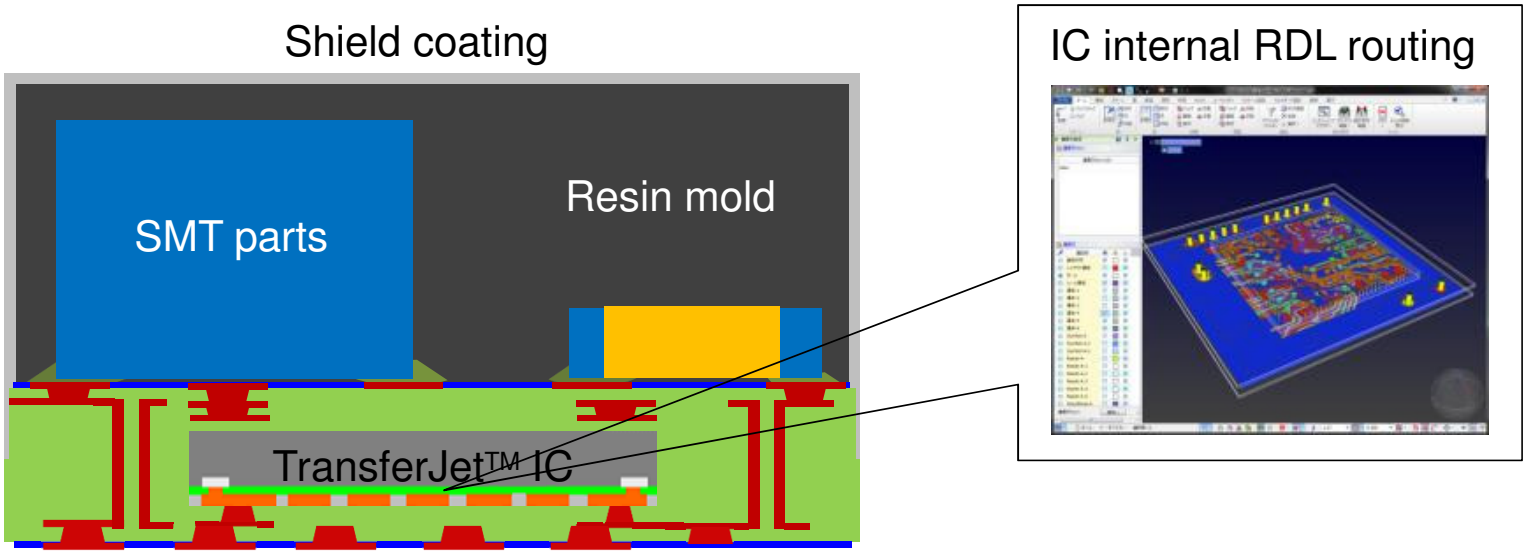
RF Matching

- Performed RF matching based on a 3-D model from inside the IC to the module terminal



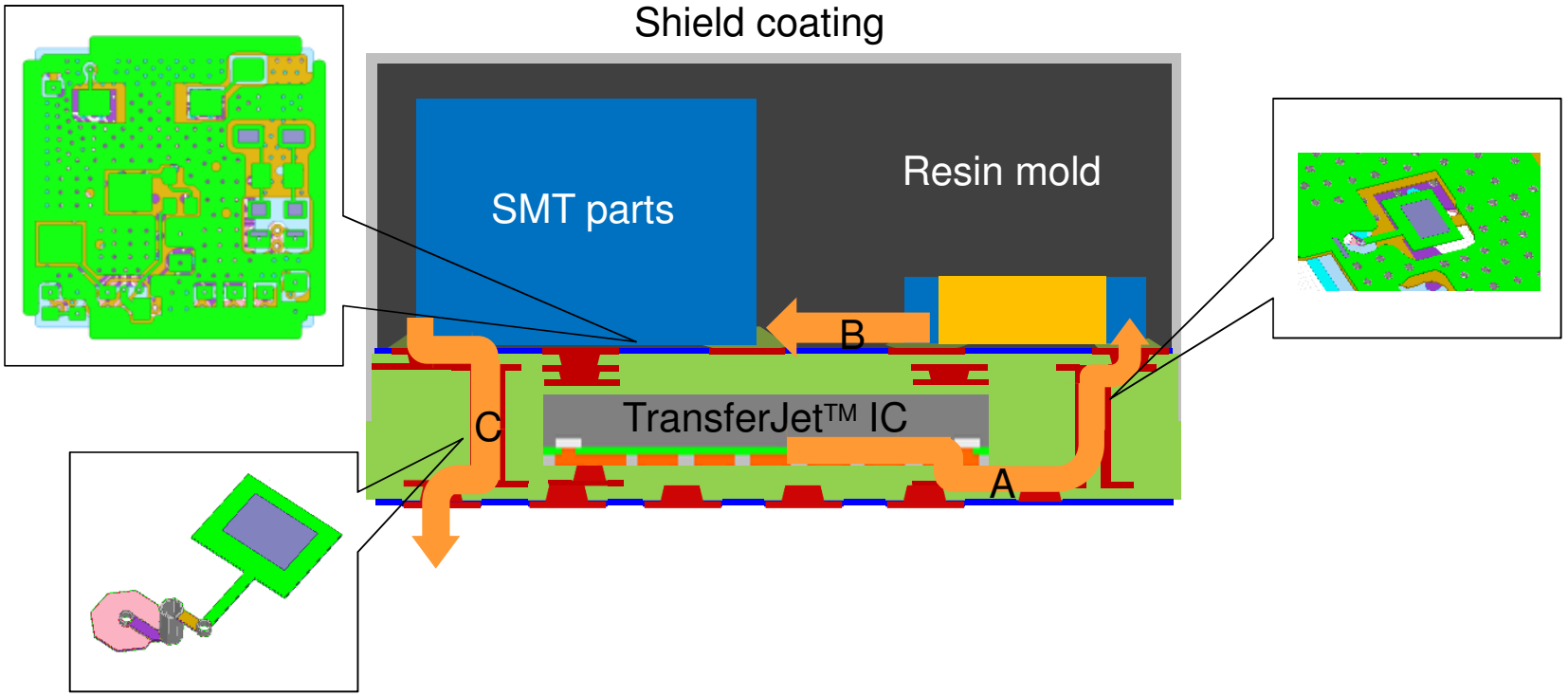
RF Matching

- Capture IC RDL routing into the module board data



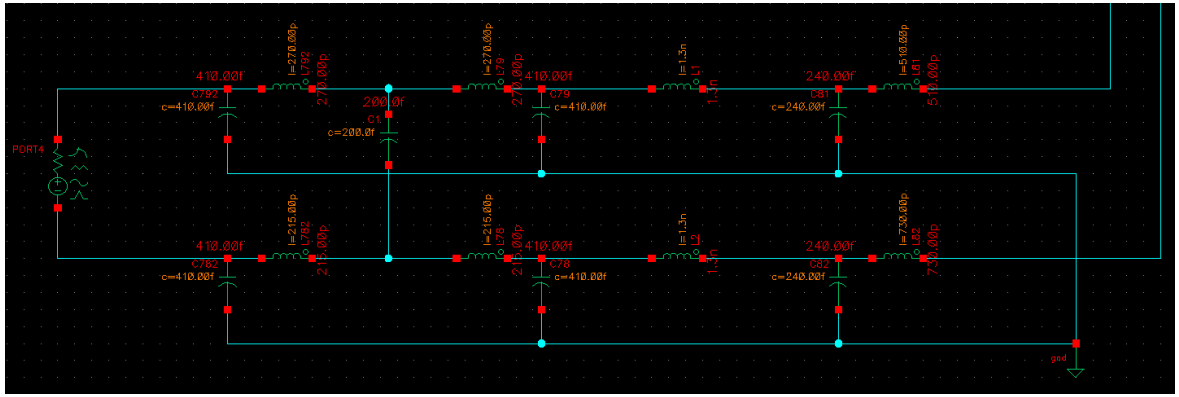
RF Matching

- Calculate L and C parasitics of each wire based on 3D model of the module. Design Force generated ANF file for Q3D

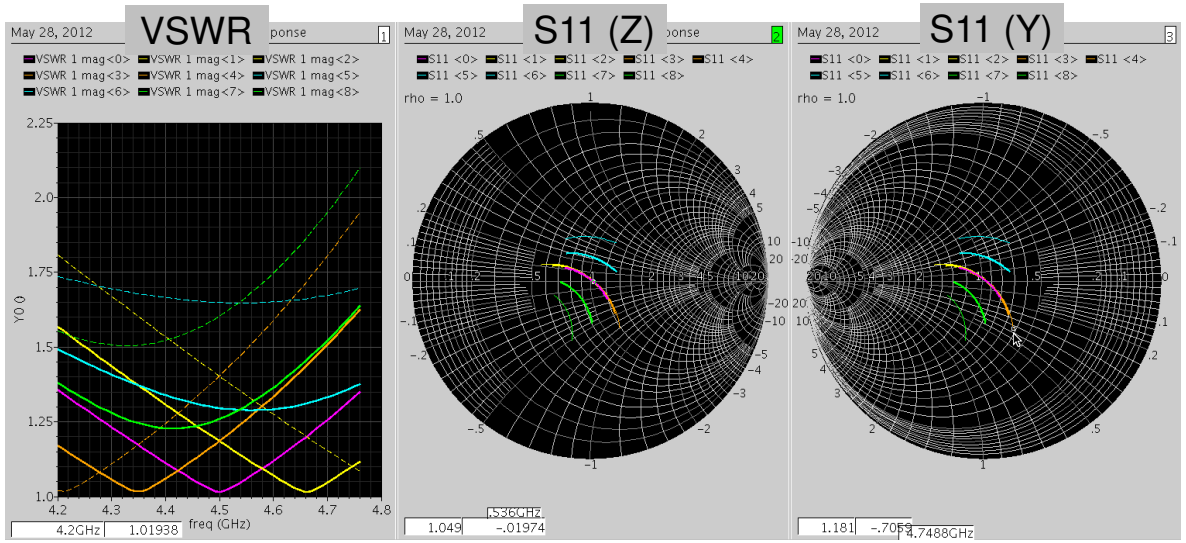


RF Matching

- Circuit simulation

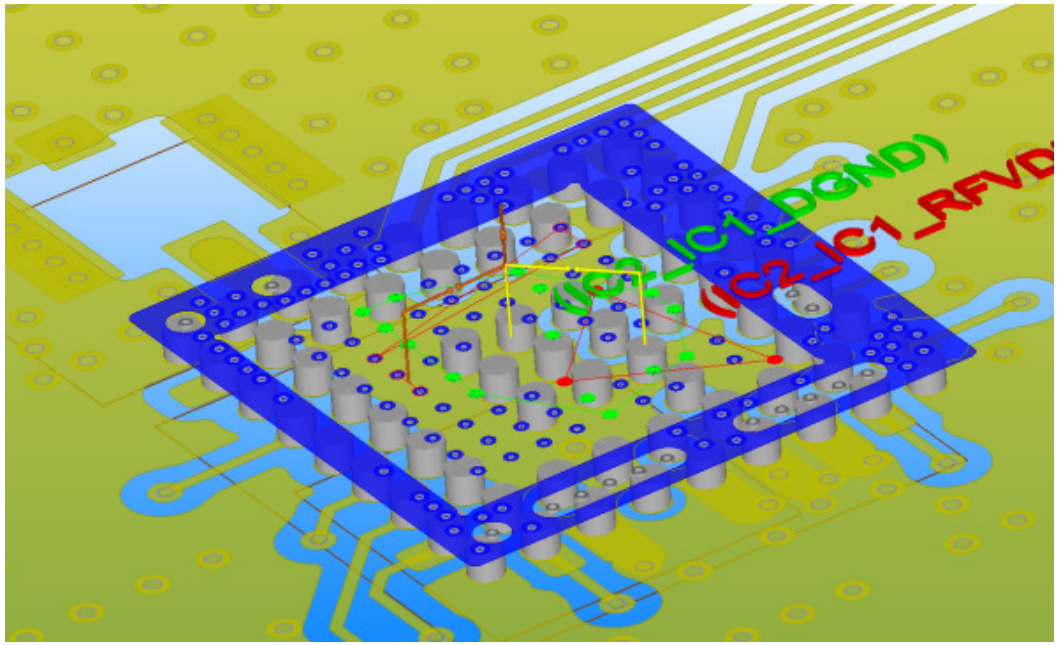


- RF match analysis



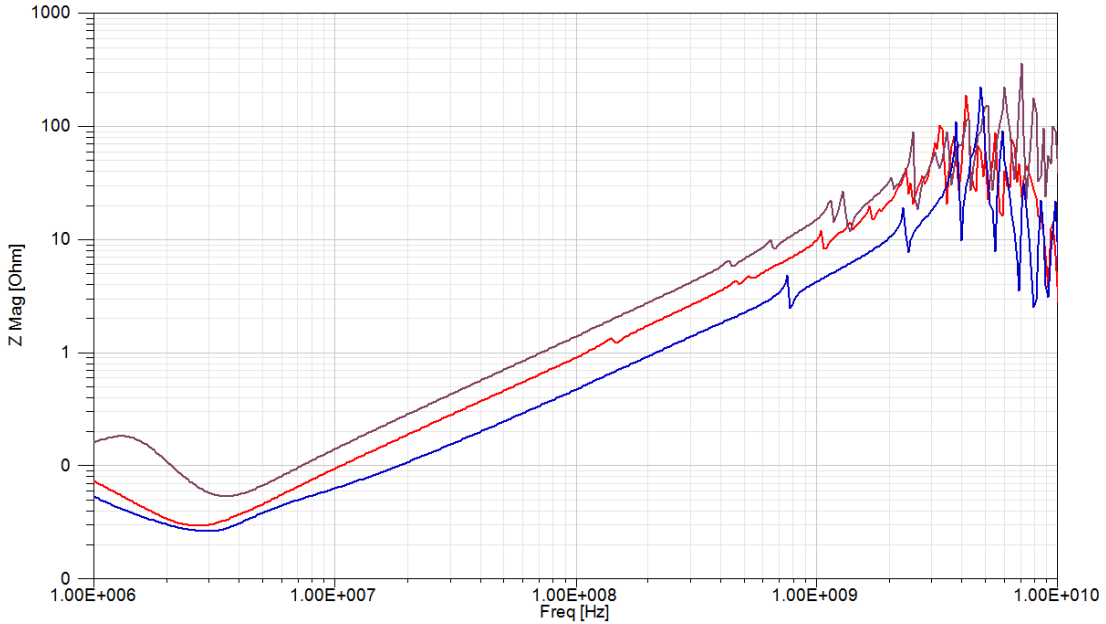
Power Stabilization

- Design Force generates ANF file for SIwave。
- A port is set for each power and ground terminal of the IC



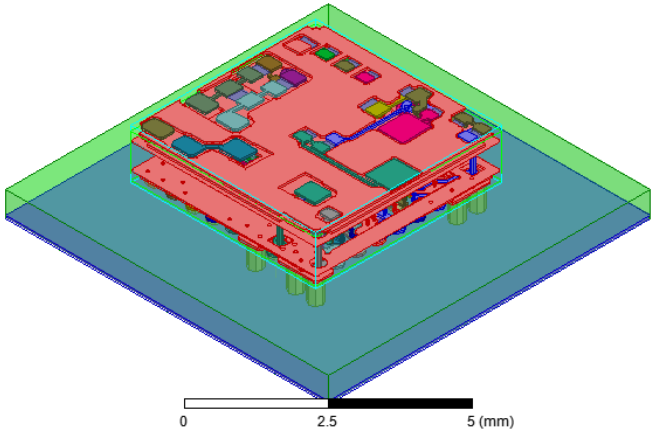
Power Stabilization

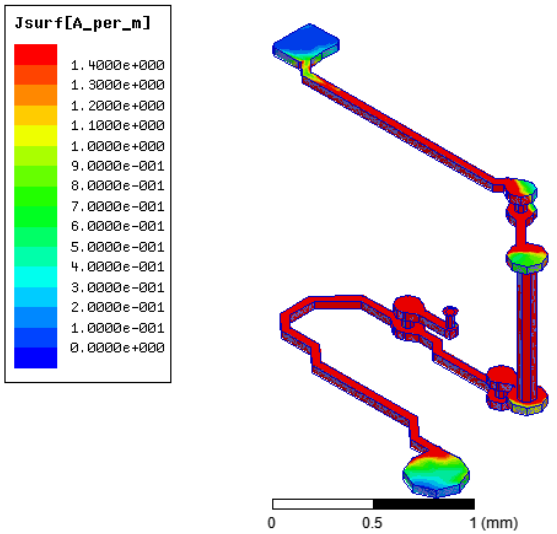
- Power/GND impedance analysis from the IC terminals,
- Calculate optimum number and value of decoupling capacitors



Minimizing Noise

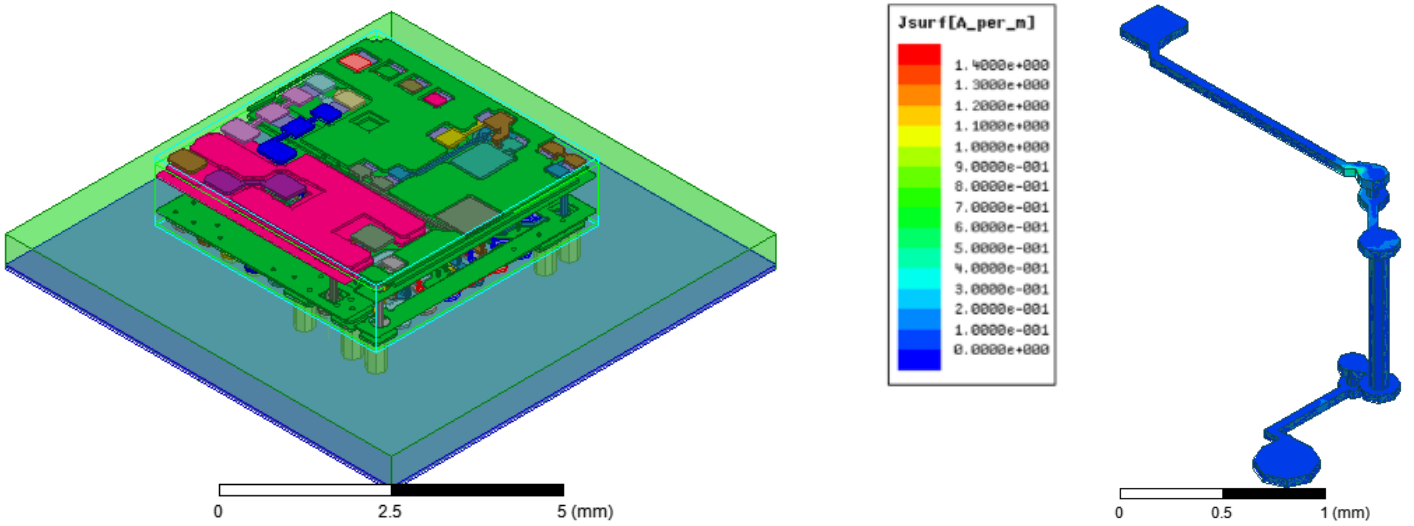
- Static resonance analysis
- Create 3D models of the module
- Performed resonance analysis.
  - Found strong resonance at 9 GHz.
  - Found the wiring causing the resonance





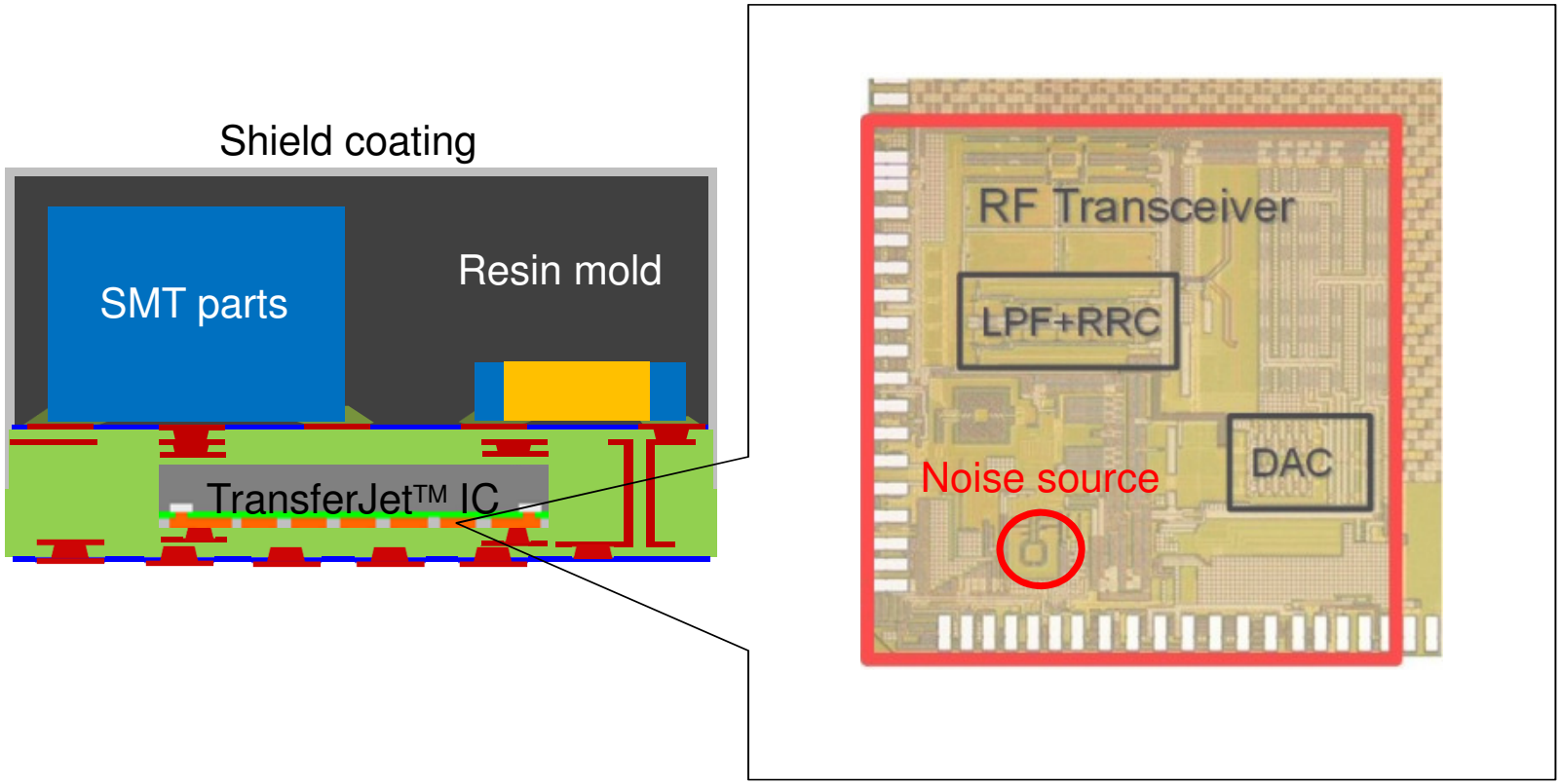
Minimizing Noise

- Corrected the resonating wiring and re-created the 3D model
- Resonance analysis confirms the problem is fixed



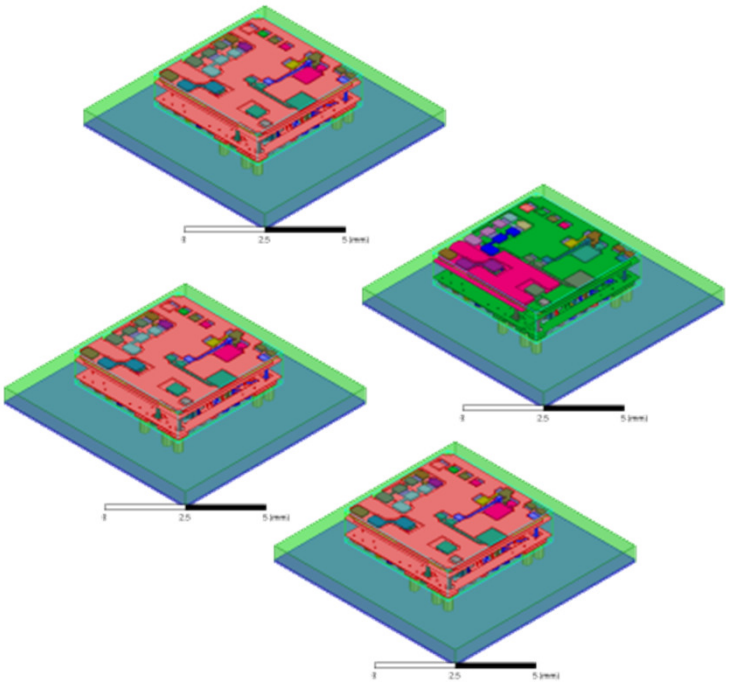
Minimizing Noise

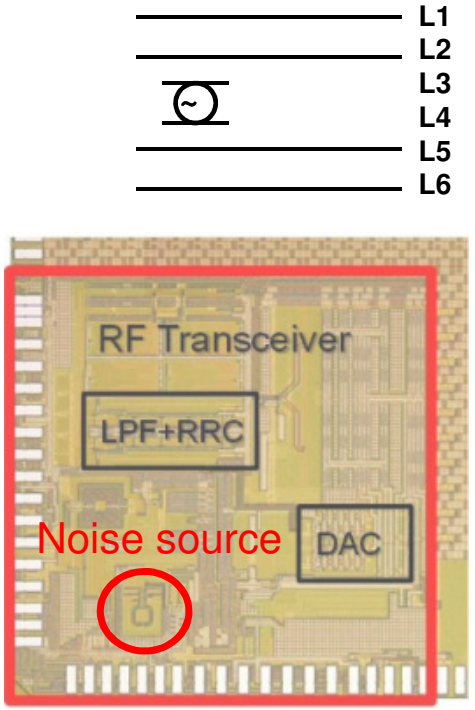
- Dynamic noise analysis



Minimizing Noise

- Explored possible solutions
- Model each solution
- Apply stimulus at the source of noise on the IC

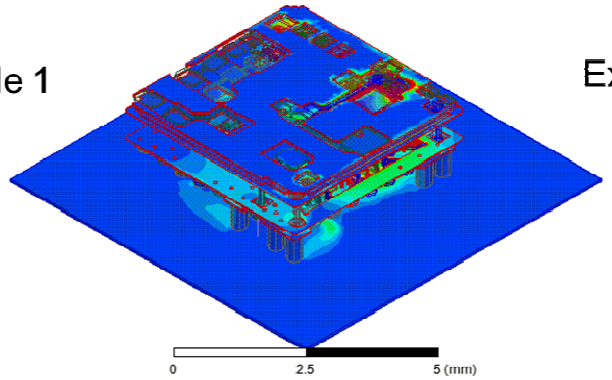




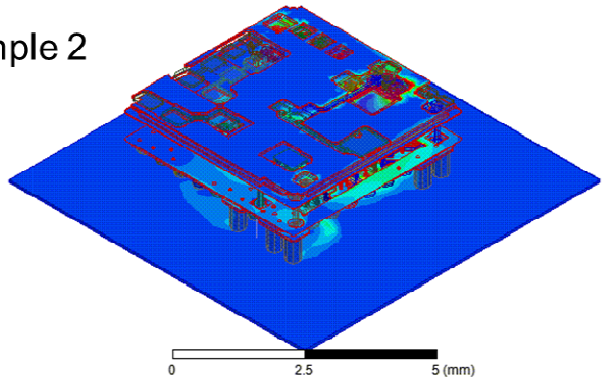
Minimizing Noise

- Repeat analysis for 30 modules

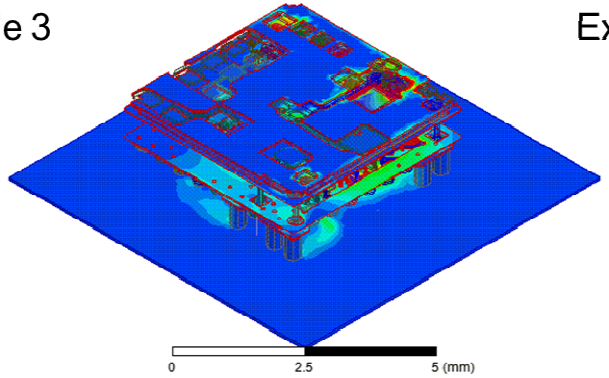
Example 1



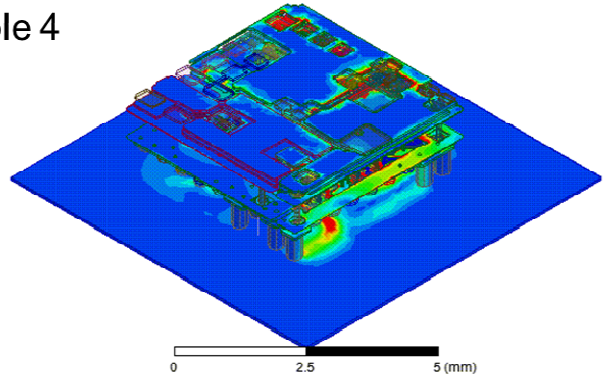
Example 2



Example 3

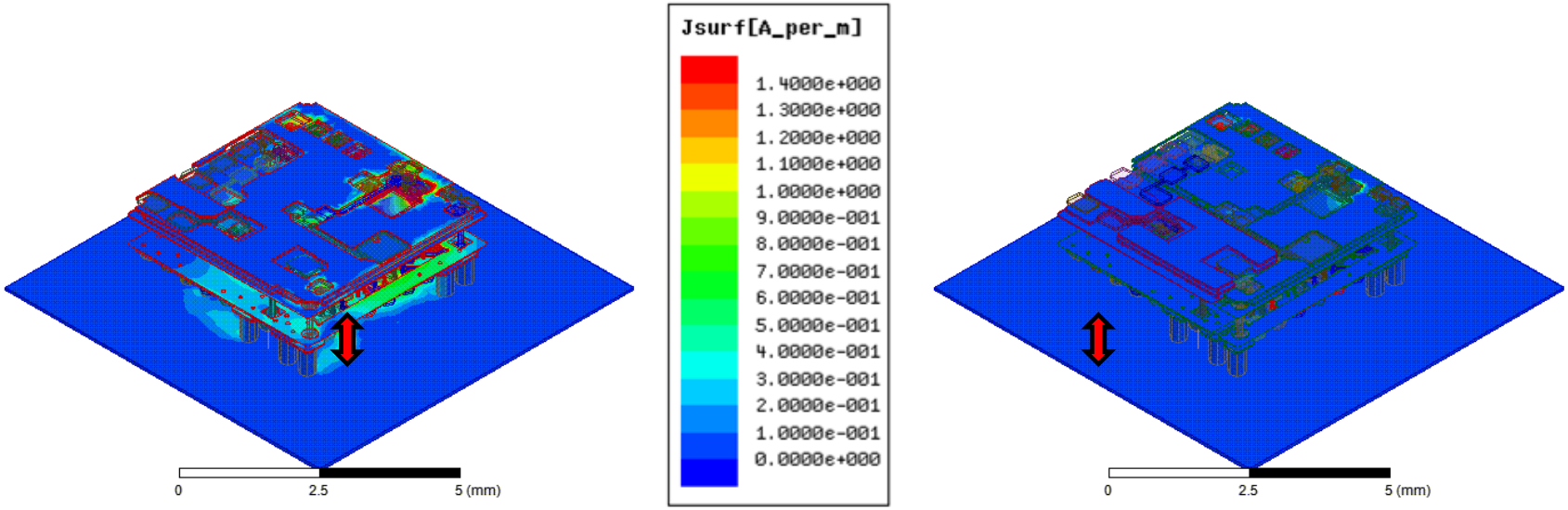


Example 4



Minimizing Noise

- Reduced noise to 1/30 of the original amount

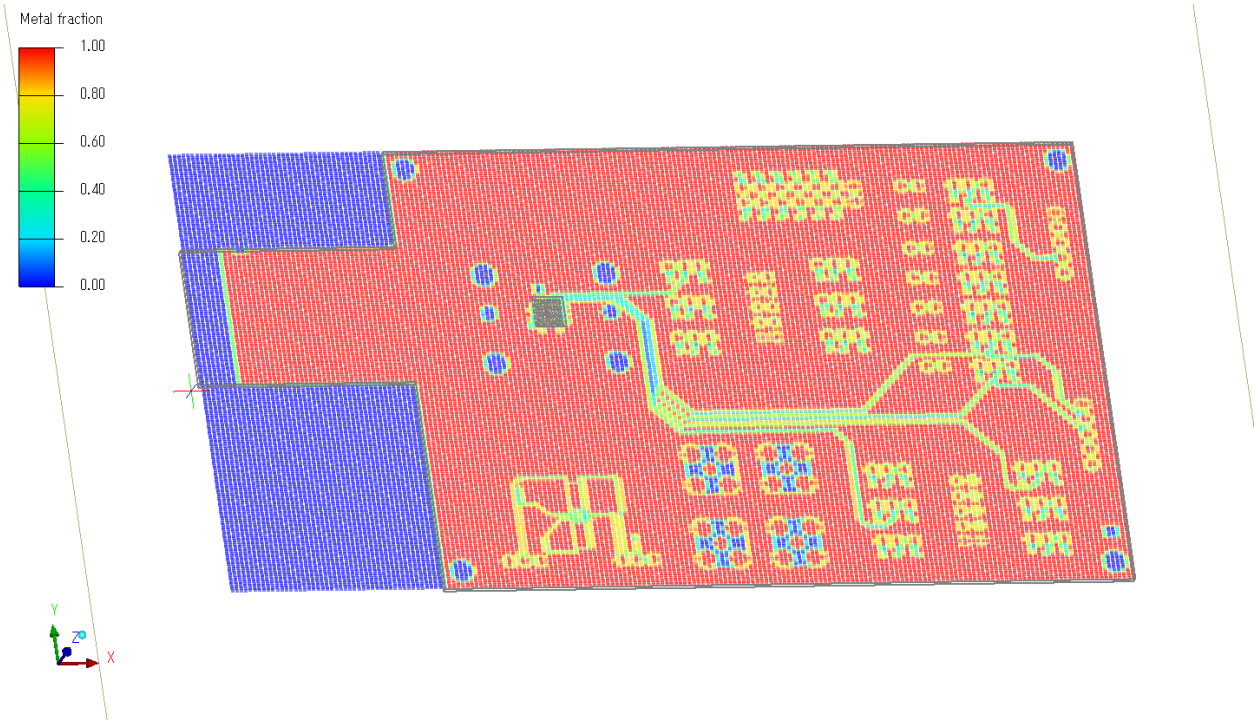


Before applying solution

After applying solution

Board-level Verification

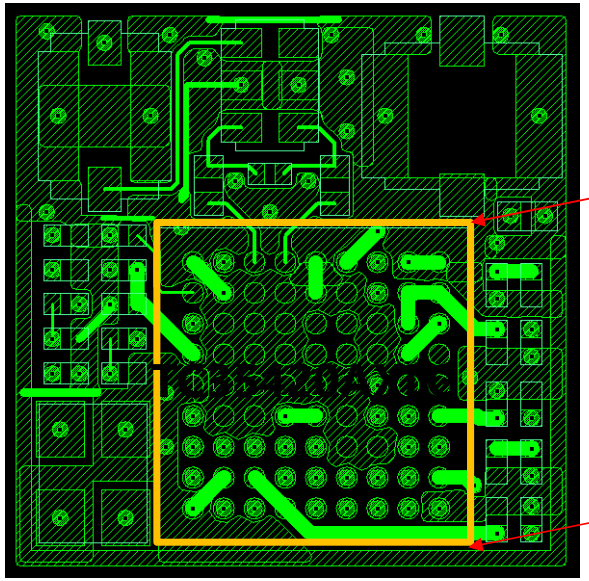
- Package level analysis results were good, so now check the module on the board
- Check the routing between the package and system board (see movie)
- Perform analysis:
  - Waveform
  - Noise
  - Thermal (see picture)



Final Results

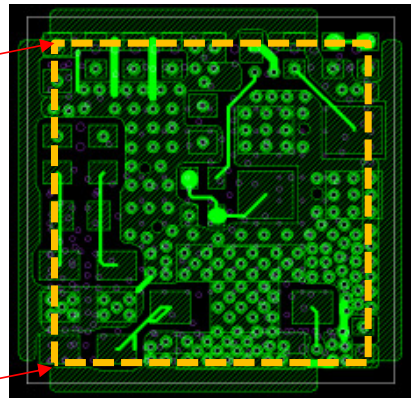
- Customer adoption of this part was made much simpler by the miniaturization to 4.8 mm square by the RF matching in the IC module.

Wireless IC + Peripheral Components

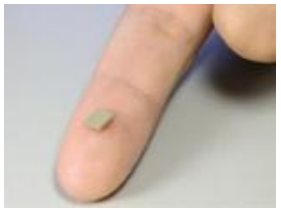


About 8mm sq.

Wireless IC Module



4.8mm sq.

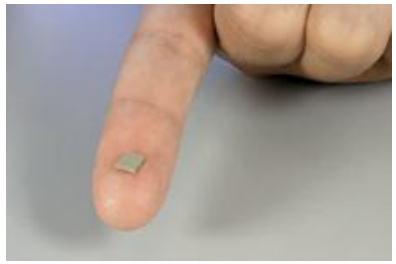


Summary

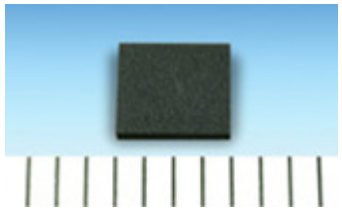
- ✓ Design Force enabled doing the design in 3D or 2D as needed throughout the design process
  - ✓ This greatly simplified the design process
- ✓ Design Force enabled routing and analysis using the technology and rules of each design space (chip, package, board)
- ✓ IC design readily imported to Design Force through LEF/DEF
- ✓ Close integration between Design Force and Ansys tools simplified the analysis process
  - ✓ Analysis of the three-dimensional structures were indispensable for the module design (especially for the RF module)
- ✓ Design Force is the only tool which can integrate the semiconductor, package, and PCB designs strongly, and it enabled the successful creation of the TransferJet ™ module.

Toshiba TransferJet™ compatible product Lineup...

Implemented products...



Transmit /
receive module



Wireless IC

Accessory products...

USB adapter module
MicroUSB adapter module
Lightning adapter module

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