eCADSTAR™

DATASHEET

SIGNAL INTEGRITY

High-speed signals must arrive in good shape, but the benefits of optimal signal integrity go further. A board with good signal integrity is more resistant to external noise and less likely to consume excess power.

To get the best results with anything you produce, you build quality into your design process from start to finish. Good-quality signals are no exception to this golden rule.

You can plan and check signal integrity at any stage from schematic to PCB layout. Wherever you do that, the results are presented the same way and the look and feel are the same.

WHAT SIGNAL INTEGRITY ANALYSIS ADDS TO eCADSTAR

- However carefully we follow rules, it's all too easy to miss something important. Maybe a signal has been ploughed through a reference plane area or a differential pair has accidentally become unbalanced.
- Signal integrity analysis reveals the truth.
- An optimized design is much better than one that just works to specification .
- More resistant to unexpected interference, environmental issues and excess power consumption .
- And when you're pushing density or performance envelopes – and let's face it, often you are – first-class signal integrity is essential.

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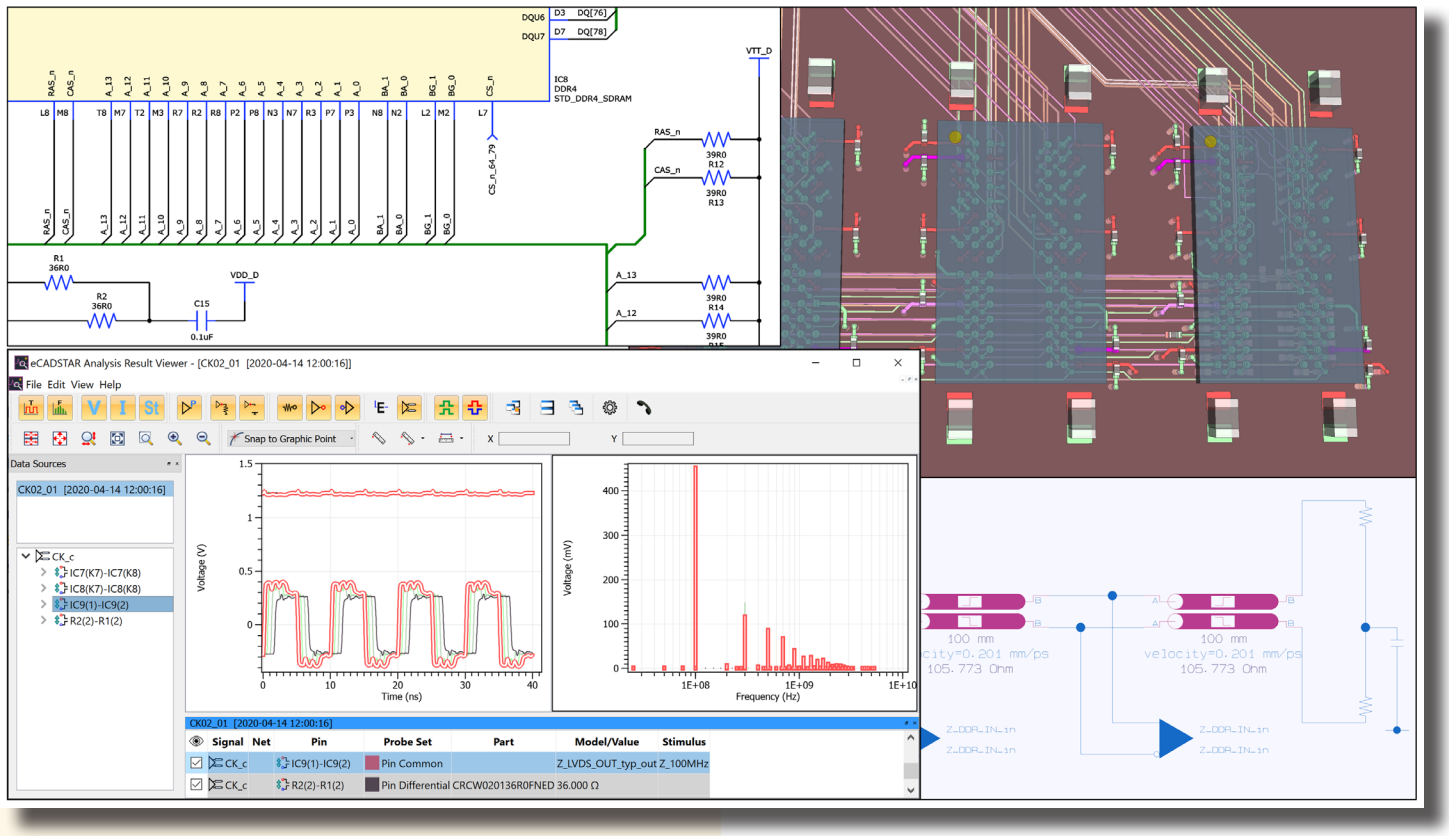


FIGURE 1: Clear, consistent results, presented the same way from initial schematic to final PCB layout

YOU CAN...

- Plan impedance-controlled PCBs, avoiding external-tool transcription errors.
  - Built-in field solver considering etch factor, partial reference planes and other detailed parameters.
- Plan high-speed topologies, avoiding predictable glitches, over-engineering and excess power consumption.
  - Simulate proposed topologies with different components, drive strengths, etc. as scenarios, selecting for optimal performance and power consumption.
  - Share your scenarios with other engineers, even if they are working on different designs.
- Check that the signal integrity you wanted is the signal integrity you've got.
  - The way you simulate routed signals is identical to the way you do it before you've even routed a track.
  - Compare results for proposed topologies, schematic signals and PCB signals in **Analysis Results Viewer** – the same look and feel in Schematic Editor and PCB Editor.
  - If you find you need to change a component or value, no problem – just change it on the schematic, forward-annotate and check again.
- Browse, import, export and share simulation models.
  - The same methods and user interface are used throughout eCADSTAR.

EXTRACT, EDIT AND SIMULATE HIGH-SPEED TOPOLOGIES

Draw any coupled or uncoupled topology and then simulate it to see how it performs. For example, plan the layout of a differential clock signal. You can sweep length, passive component values and other parameters to achieve optimum signal integrity.

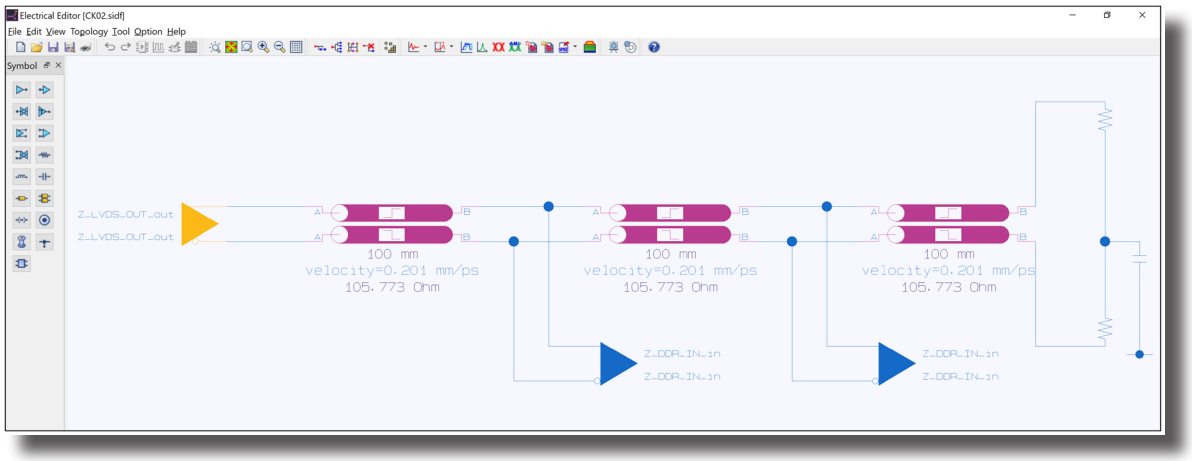


FIGURE 2: Scenario for a differential clock layout

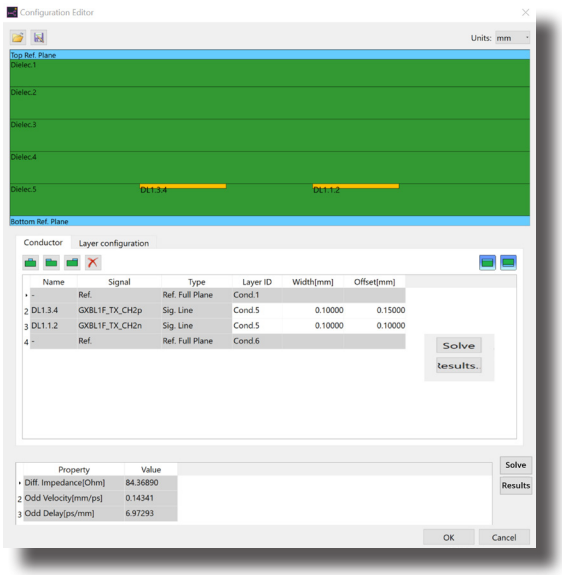


FIGURE 3: Extract, draw and edit track configurations

Solve track configurations like this coupled pair. As with high-speed topology, these configurations can be extracted from physical layout, created by you or edited, to find the effects of different choices. In the example shown here, differential impedance would guide the choice of a bridging terminator at the receiver, while odd-mode impedance would guide the values of separate shunt resistors to a voltage in the same positions. You could then simulate with these values to make sure.

Simulate from Constraint Browser, Electrical Editor or directly from the eCADSTAR PCB canvas, with or without coupling. The same simulation and result viewer are used throughout eCADSTAR, so there's just one user interface to learn.

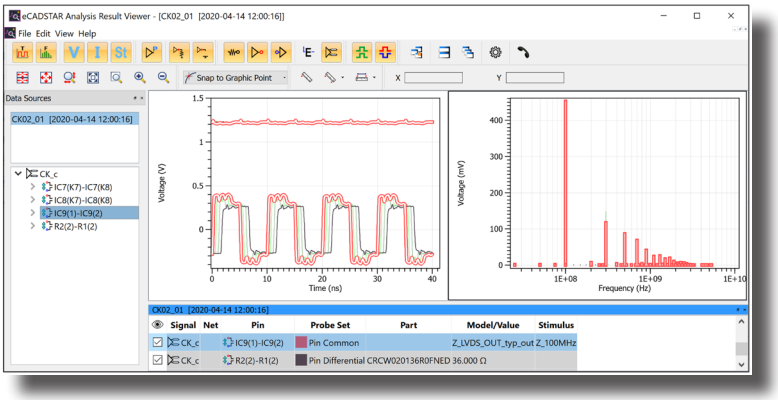


FIGURE 4: Analysis Result Viewer

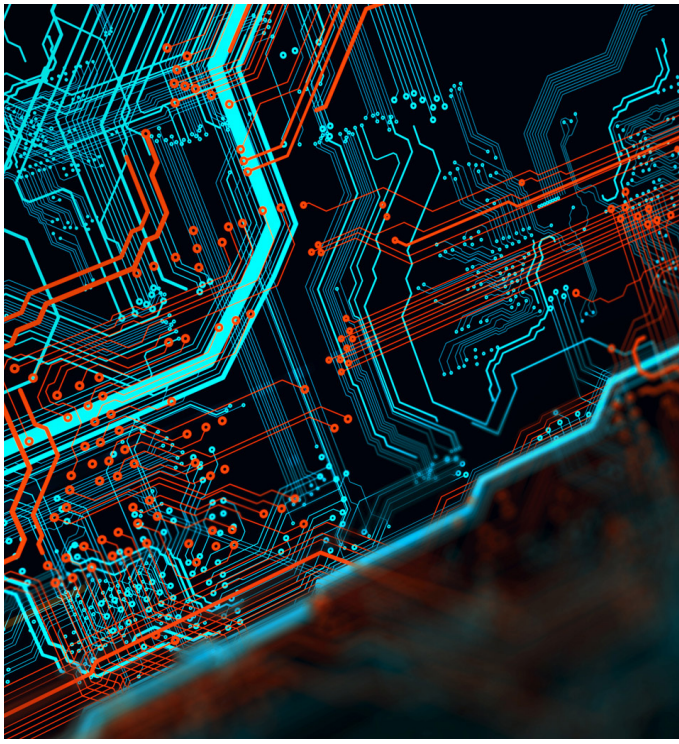
VIEW AND MEASURE WITH COMPREHENSIVE OPTIONS

Time domain voltage and current waveforms to assess basic signal integrity.

Frequency domain and phase plots to identify high-amplitude frequencies that could cause EMC issues.

Customizable probes and measurements to get quantified numerical results, including overshoot, undershoot, thresholds and many others to provide all the detail you need to drill down to specifics.

Ability to save and compare results with other simulations.



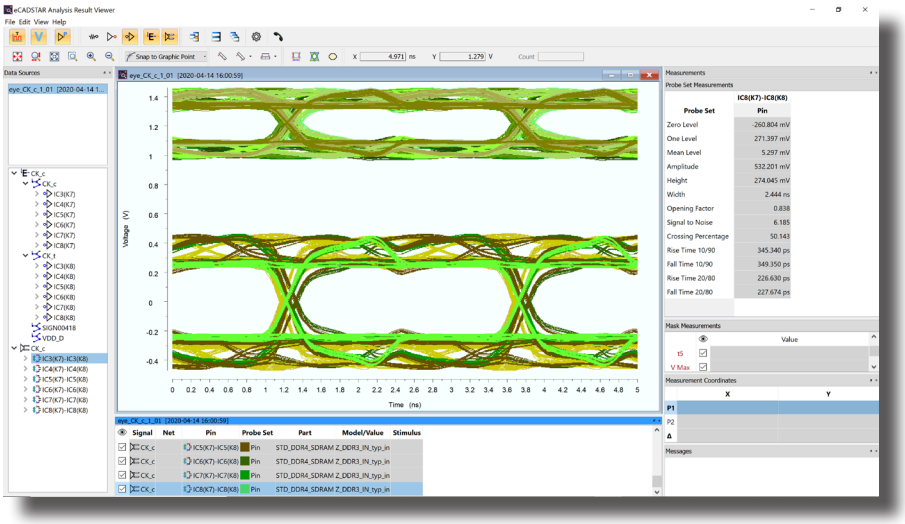


FIGURE 5: Eye pattern analysis

CHECK EYE PATTERNS

At really high speeds, waveforms are not enough. Key parameters have to be quantified, as well as verifying the eye opening. Selectable standard stimulus patterns include 8b/10b encoding or you can create your own and save them to use in any design.

KEEP SIMULATION LIBRARIES ORGANIZED

Import and verify IBIS and other model formats. Browse models the same way in PCB Editor and Schematic Editor. Assign models to components in a straightforward table style in Constraint Browser. Export, import and share models with other engineers.

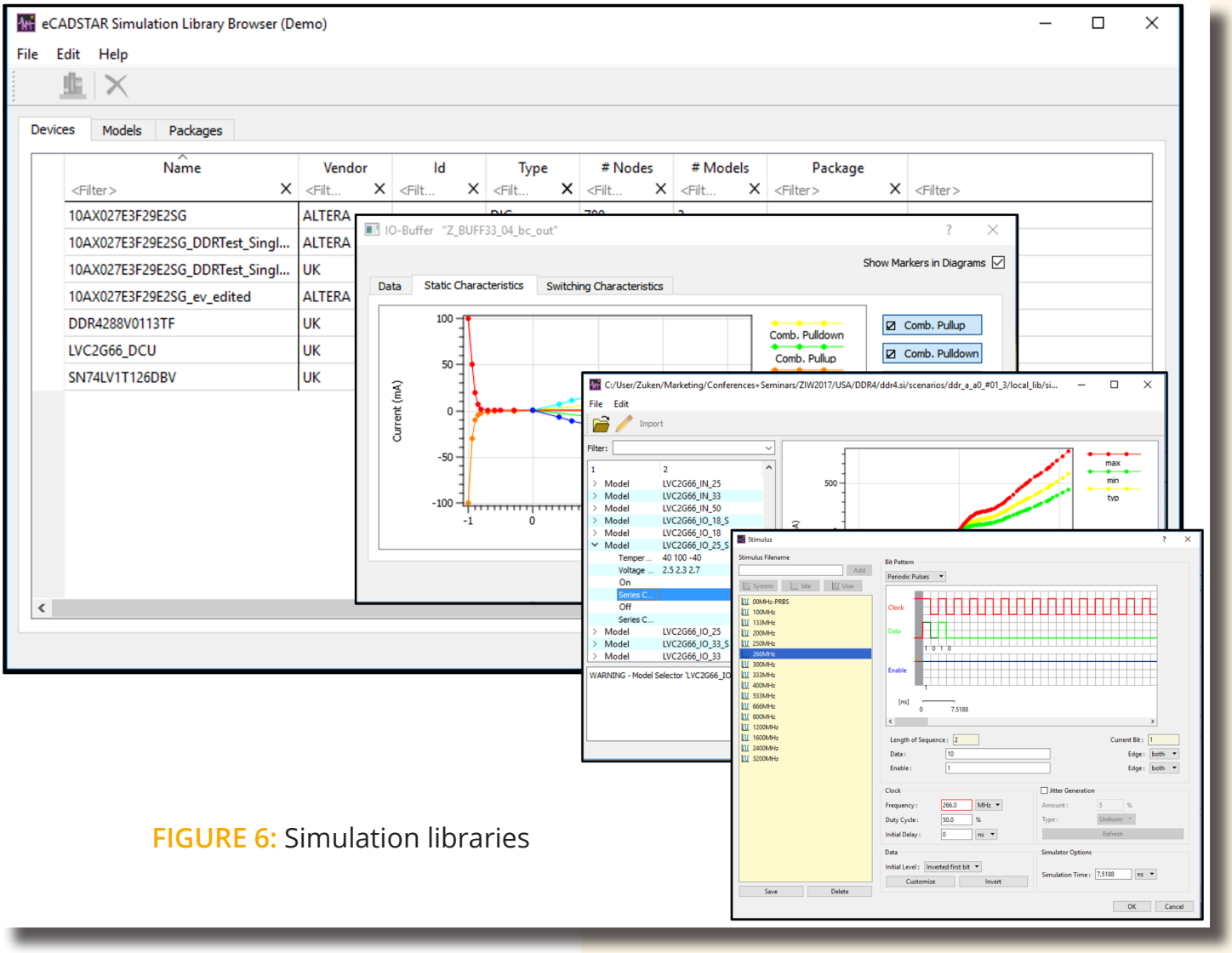


FIGURE 6: Simulation libraries

AND IF YOU ADD SIGNAL INTEGRITY ADVANCED...

- Generate data for external simulators.
  - Export S-Parameter models.
- Simulate to locate and quantify discontinuities.
  - Perform TDR (Time Domain Reflectometer) style analysis.
- Export to HSPICE for detailed, transistor-level simulation.

ADD-INS FOR ULTRA-HIGH-SPEED SIGNALS

Go Advanced. You can add cost options to analyze ultrafast signals.

- S-Parameter export to create models for other simulators.

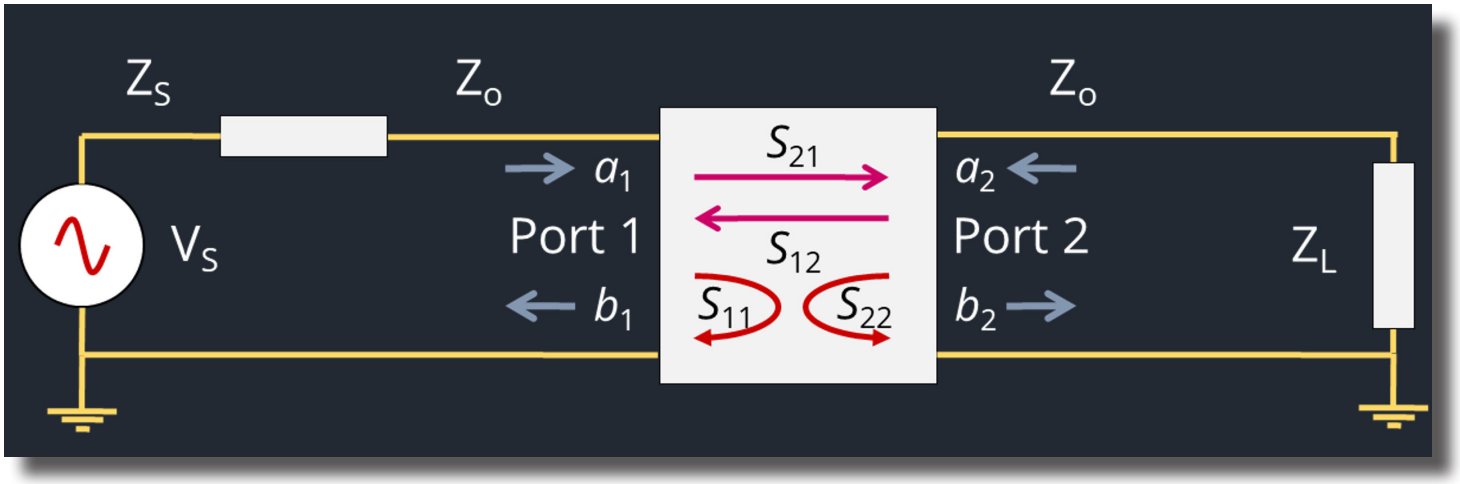


FIGURE 7: S-Parameter model - conceptual illustration

- Time-Domain Reflectometer (TDR) style simulation to locate and measure signal path discontinuities in detail.

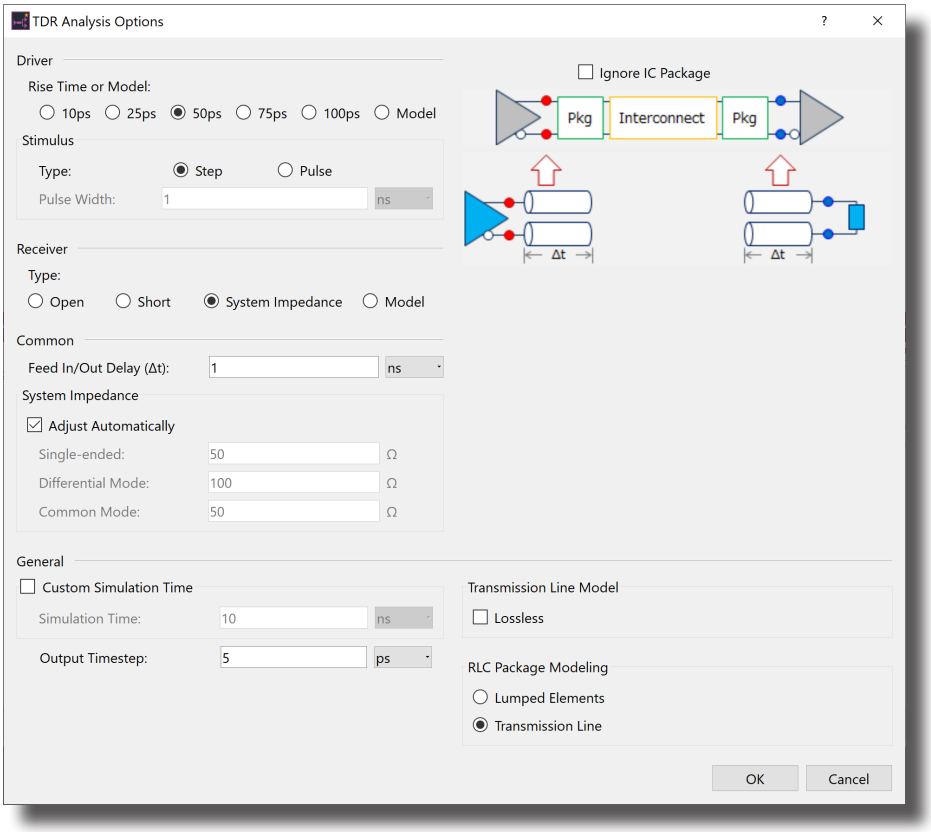


FIGURE 8: Detailed TDR analysis setup

- Export to HSPICE simulation to simulate at transistor level, considering detailed internal active device behavior.