dirror mod.use\_y wirror mod.use z = False elif \_operation == "MIRROR Z": mirror\_mod.use x = False mirror\_mod.use y = False mirror mod.use z

## **ecadst**AR<sup>™</sup>

DATASHEET

# **POWER INTEGRITY**

Power integrity (PI) and EMI issues sometimes only reveal WHY WOULD YOU NEED PI themselves right at the end of testing - or even worse, in AND EMI ANALYSIS? the field.

Causes can be subtle, but you can avoid a lot of PI and EMI trouble with eCADSTAR Power Integrity and EMI Analysis.

### www.ecadstar.com

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 It is easy to miss a serious power integrity or EMI issue. This can be as simple as using the wrong kind of via to take power from one layer to another or as subtle as a local resonance that stops I/O getting enough switching power. Analysis can be as shallow or deep as you wish. Even the most straightforward DC analysis often throws up a surprise.

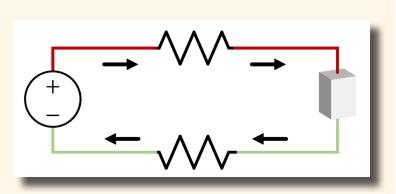
• For effective design reviews, you need evidence. PI and EMI analysis runs produce results presented in a consistent way.

 More and more PCBs are mixed-technology and that means careful power distribution layout. RF connectivity, controllers and noisesensitive analog I/O need careful design to coexist effective on the PCB.

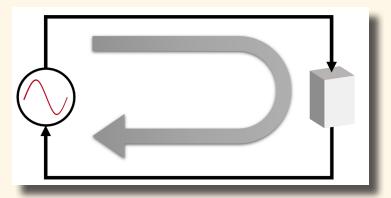
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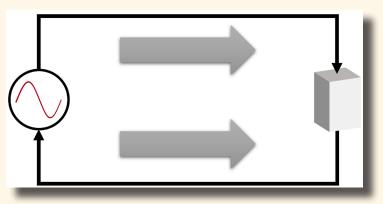
Although the calculations are sophisticated, the PI and EMI analysis deals with three basic issues:



DC voltage drop and potential sources of AC noise on power buses.



Differential-mode EMI caused by current flowing in loops, including signal and return loops.



Common-mode EMI caused by current flowing in the same direction – for instance where PCB structures create unintended antennas.

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### **POWER INTEGRITY (PI)**

Configurable controllers, sensors, Internet of Things (IOT) and many other technologies demand careful power distribution. Problems can easily get missed – not just DC, but subtle issues that involve electromagnetic coupling.

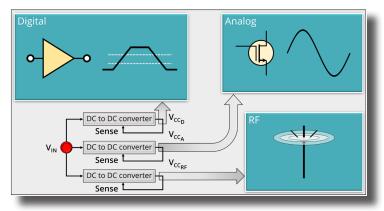


FIGURE 1: Conceptual diagram of power distribution on an IOT board

### **DC POWER INTEGRITY**

The first thing to check is DC stability. Current flows from power sources to component power inputs and then back where it came from, so the question is, do those components get a good, solid supply voltage and a good ground return path?

Current might have to squeeze through narrow conductors or through undersized vias or travel around obstacles. Different components consume different amounts of power. Current that takes a detour meets more resistance - and more resistance means a voltage drop between power supply and IC.

The concept is quite simple, but supply current follows intricate paths. You need to know that adequate power gets to all devices. Minimizing power voltage drop also makes designs more resistant to noise and optimizes I/O performance.

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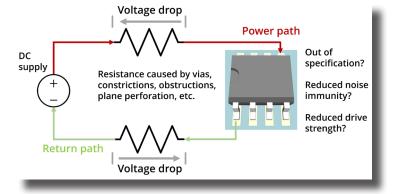


FIGURE 2: Power and return paths are different for each device

It's easy to introduce obstacles by accident while you're laying out your design.

Each power supply source and return pair is call a Power Bus. The first thing to check is that all the power buses are recognized correctly. It's easy to adjust them to make sure.

Even before producing detailed DC results, DC analysis detects hard discontinuities in power distribution like the one shown in Figure 3.

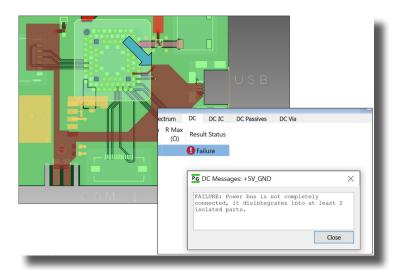


FIGURE 3: This via did not span enough layers to carry +5V to the IC (blue arrow added for illustration)

Once you know a whole power bus and its return are at least connected, you can get all the details you need from DC Analysis. The more information you provide, the more detail you can get. Basic component information comes from the same simulation library used by eCADSTAR signal integrity simulation, but you can add more in categorization, to refine your results and adjust values for what-if analysis.

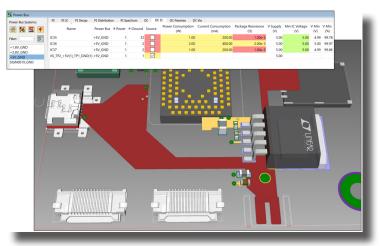


FIGURE 4: DC analysis returns detailed results for all components and objects

DC analysis results include:

Resistance analysis.

- Voltage distribution.
- •Voltage (IR) drop analysis.
- •Power distribution via performance, including current and IR drop.

•Voltage and current distribution heatmap displayed directly on PCB Editor canvas.

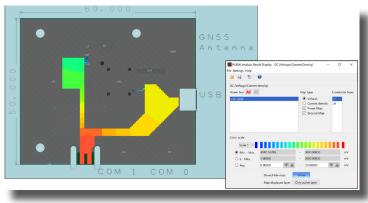


FIGURE 5: Voltage and current density maps are displayed directly in PCB Editor



#### AC POWER INTEGRITY

Even if we know DC power is getting to all devices in good shape, is the same true when the design is running at full speed? A good power distribution is low-impedance, not just low-resistance. For low-impedance power distribution, capacitance is our friend and inductance is our adversary. Even capacitors can become inductors unless we choose them wisely, when the effects of their packaging dominate their apparent capacitance at high frequencies.

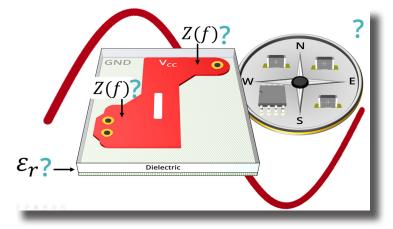


FIGURE 6: eCADSTAR Power Integrity analysis helps to determine capacitor type/location and layer stack dimensions and materials

#### Results include:

•Impedance analysis.

High impedance "hot spot" identification.
Power impedance heatmap, displayed directly in eCADSTAR PCB Editor.

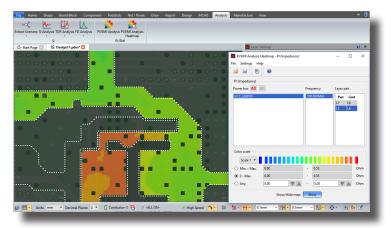
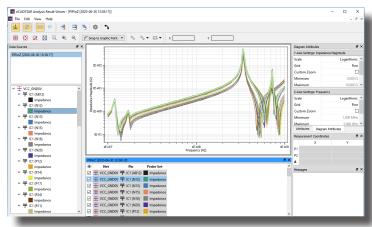


FIGURE 7: Power impedance heatmap style for a Vcc plane

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•Resonance at specified locations at specified frequencies.



## FIGURE 8: Impedance plot for a point on a power plane

•Decoupling capacitor effectiveness analysis with what-if capability for alternative decoupling capacitors (different type, value, position), reducing the number of decoupling capacitors or adding virtual ones.

wer Bus Systems:	PI	PI IC PI D	ecap PI Distrib		PI Spectru		DC DC IC	DC Passives	DC Via				
1 🔀 🦉	Name	Power Bus	Parasitic Model	C in (pF)	ESR (Ω)	ESL (nH)	Inductance (nH)	Resonance (MHz)	Effectiveness	Nearest IC	X Position (mm)	Y Posit (mn	
er: 🔤 📘	⊠C2	+5V_GND	0603	10000.00	0.10	0.45	1.27	44.58 M	ounting ineffective	]IC1	15.89		8.9
	⊡c3	+5V_GND	0603	10000.00	0.10	0.45	1.27	PG Decap Effe	ectiveness Info				×
1.8V_GND 3.8V_GND	<b>⊘</b> C4	+5V_GND	0402	10000.00	0.06	0.40	1.28						
SV_GND	⊡c5	+1.8V_GND	0402	10000.00	0.06	0.40	1.51	1 Properties of C2					
GIGN0019_GND								Name	C2				^
								Power-Net na	ame +5V				
								Ground-Net r	ame GND				
								Value	10000.00 pF				
								ESR	0.10 Ω				
								ESL	0.45 nH				
								Resonance (E	SL) 75.03 MHz	75.03 MHz			
								Bandwidth	34.31 MHz				
								Q	2.19				
								Status	Mounting in	Mounting ineffective, bypass capacitance O			
								L-Power	Unknown				~
										Clo	se	Help	

FIGURE 9: Identifying ineffective decoupling in power distribution

#### **EMI ANALYSIS**

Compliance to Electromagnetic Compatibility (EMC) regulations is a requirement in all major markets. Ensuring that Electromagnetic Interference (EMI) is kept as low as possible is a big part of that.

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Regulations also cover susceptibility to external interference. Actions taken to keep EMI low usually help reduce susceptibility too, because of the electromagnetic reciprocity. EMI results are presented in the same Analysis Result Viewer (ARV) as those for Power Integrity or Signal Integrity. Just as with Power Integrity, you can visualize results in heatmap-style directly in eCADSTAR PCB Editor.

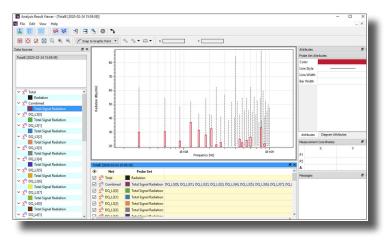
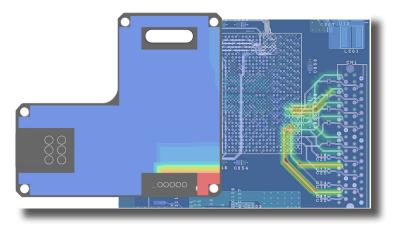
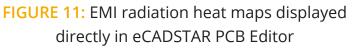


FIGURE 10: Numerical results for EMI radiation





### QUANTIFIED RESULTS IN THE SAME ANALYSIS RESULT VIEWER USED FOR SIGNAL INTEGRITY

Why learn multiple user interfaces when you can learn just one? Where applicable, detailed results for EMI and power integrity, including plane impedance at specific coordinates and radiation at specific frequencies, are displayed in Analysis Result Viewer.



FIGURE 12: The same Analysis Result Viewer is used to display detailed signal integrity, power integrity and EMI analysis results

Power integrity and EMI analysis may seem specialized, but good power integrity and low EMI are essential to all electronic products. Just as with signal integrity the need has become greater as more - and faster - components are packed on to PCBs.

This type of analysis used to be the domain of specialists, but usually only large companies have specialists like that. You need a solution that's an integral part of PCB design - not a separate analysis package with complicated data transfer, different user interfaces and disjoint ways to view results. Power integrity and EMI analysis are designed into eCADSTAR, sharing the same design data and the same simulation library used for signal integrity - and supported by the same team.

You can cross-probe, visualize and quantify with much less room for error or misinterpretation. You can save results in convenient formats for internal and external design reviews – not just text and numbers but graphics too.